

649-M3

Rev: 1.0

Page Index

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Revision History :


1. Ver A: Modified 649-M2 from DDR to DDRII.
2. Ver 1.0: Modified voltage regulator and co-lay 655/880.

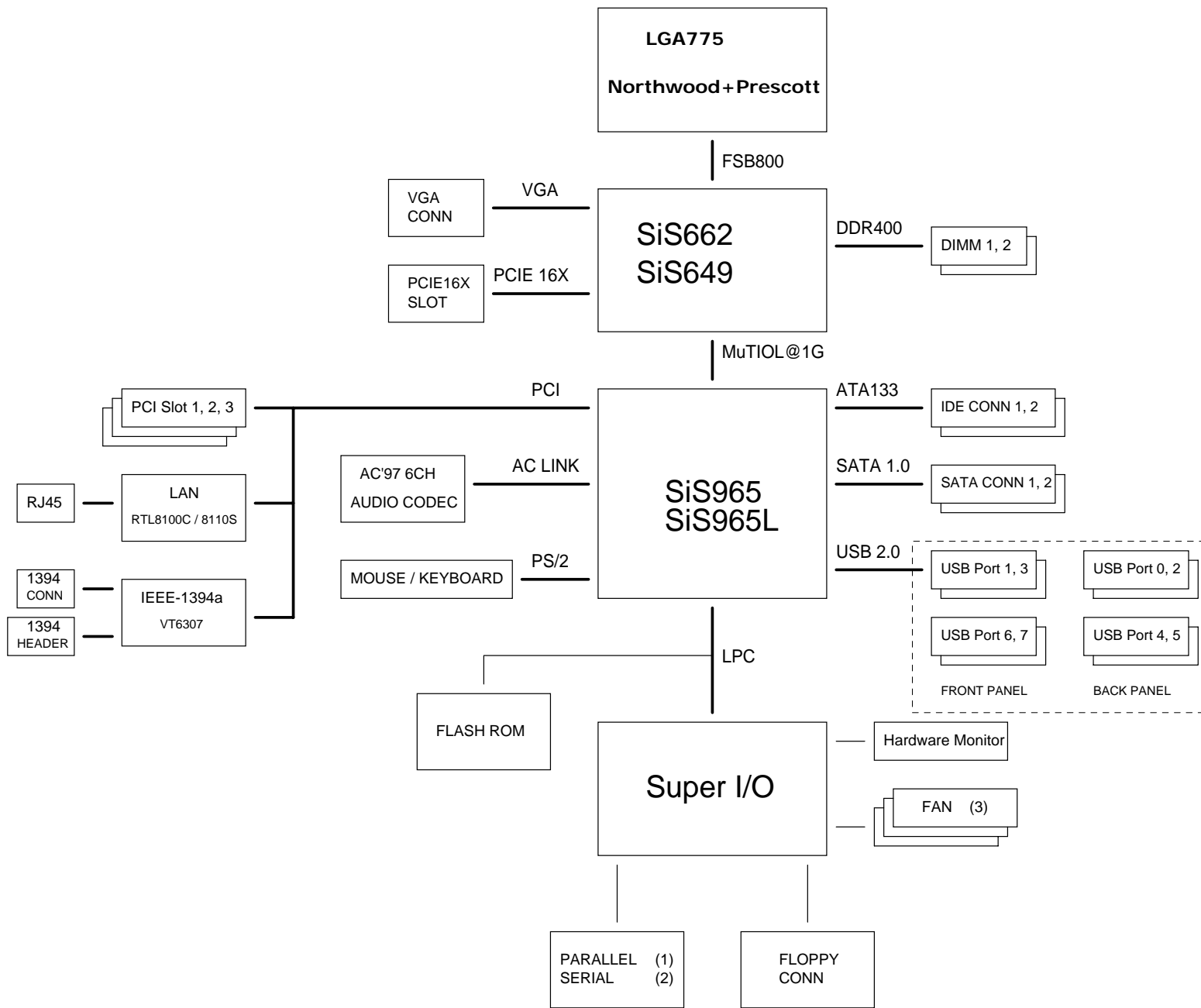
1. Cover Sheet
2. Block Diagram
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4. Socket LGA775-1
5. Socket LGA775-2
6. Socket LGA775-3
7. SiS649-1 (HOST / PCI-EX)
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9. SiS649-3 (LINK)
10. SiS649-4 (Power)
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14. SiS965-4 (Power)
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17. DDR DIMMII 1, 2
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33. DUAL 5V, 3V& SB Regulator
34. VRD10 (CPU Vcore)
35. ATX / Panel / RTC
36. BOM and GPIO Attention

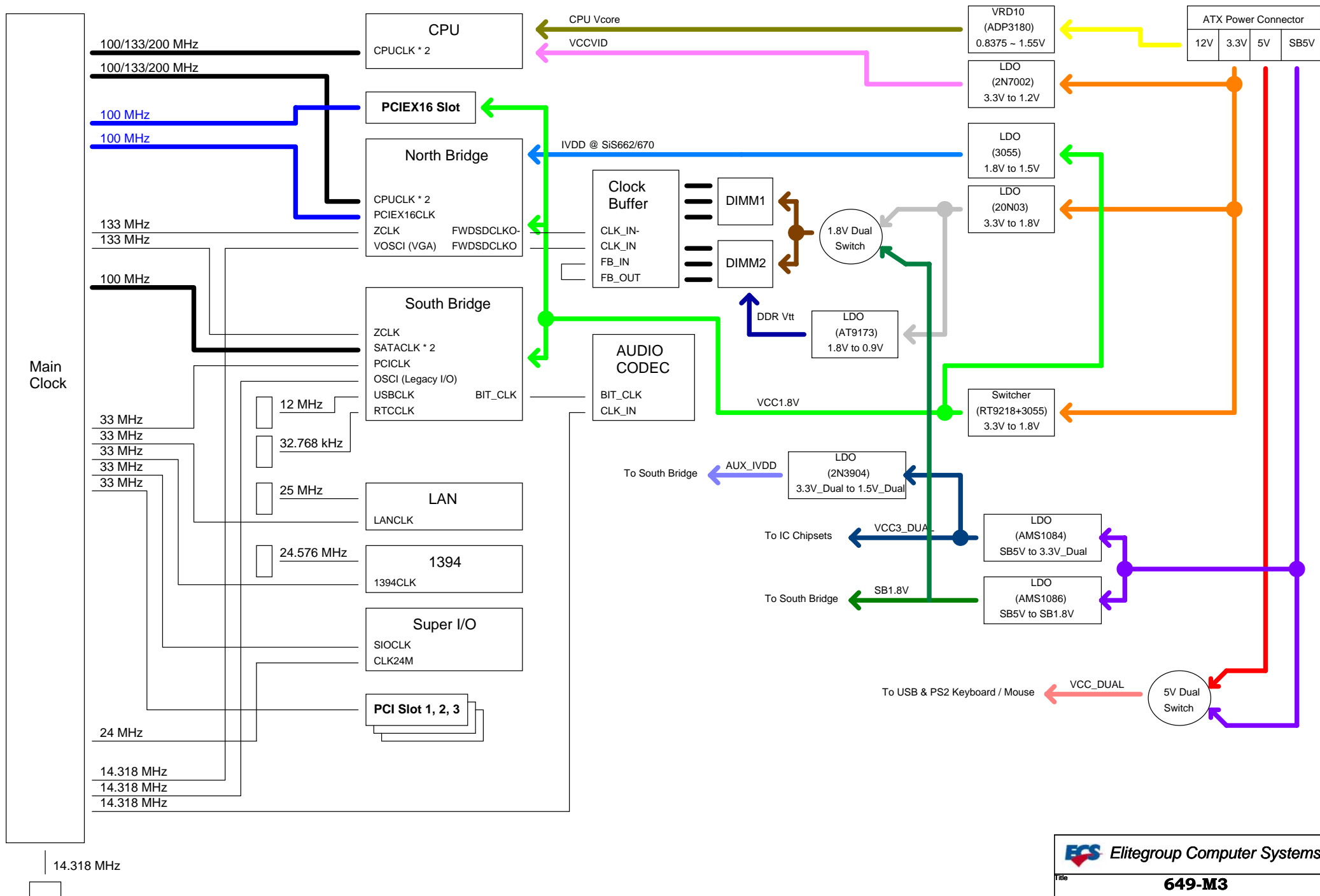
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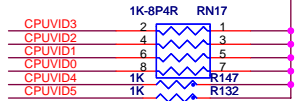
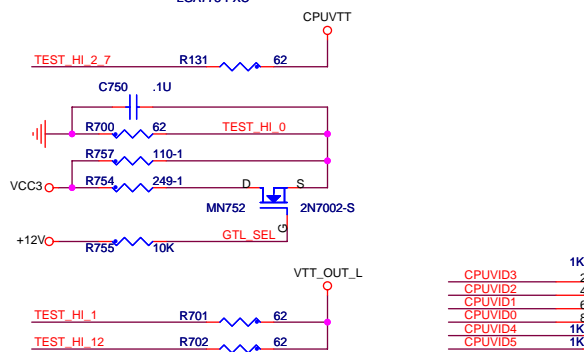
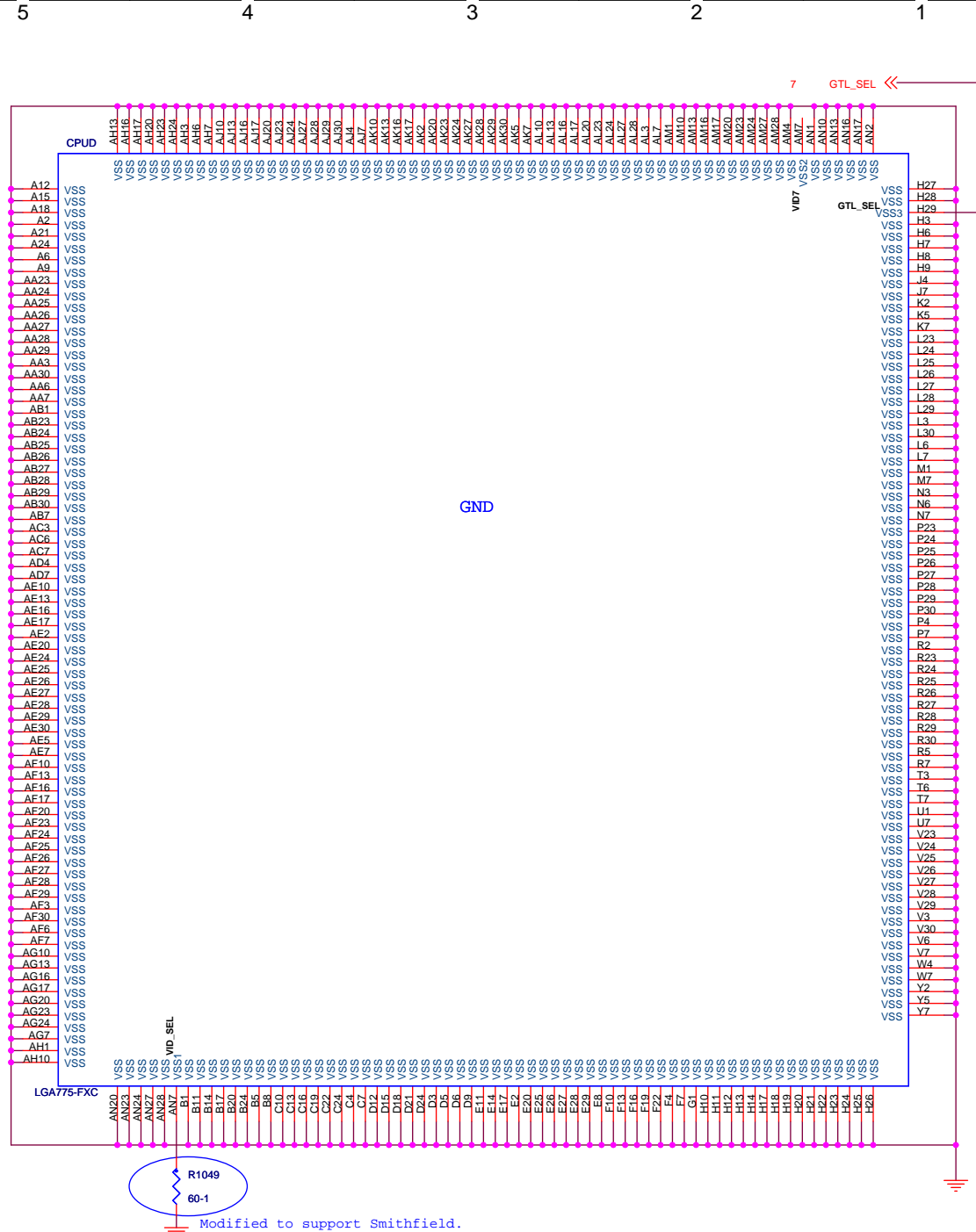
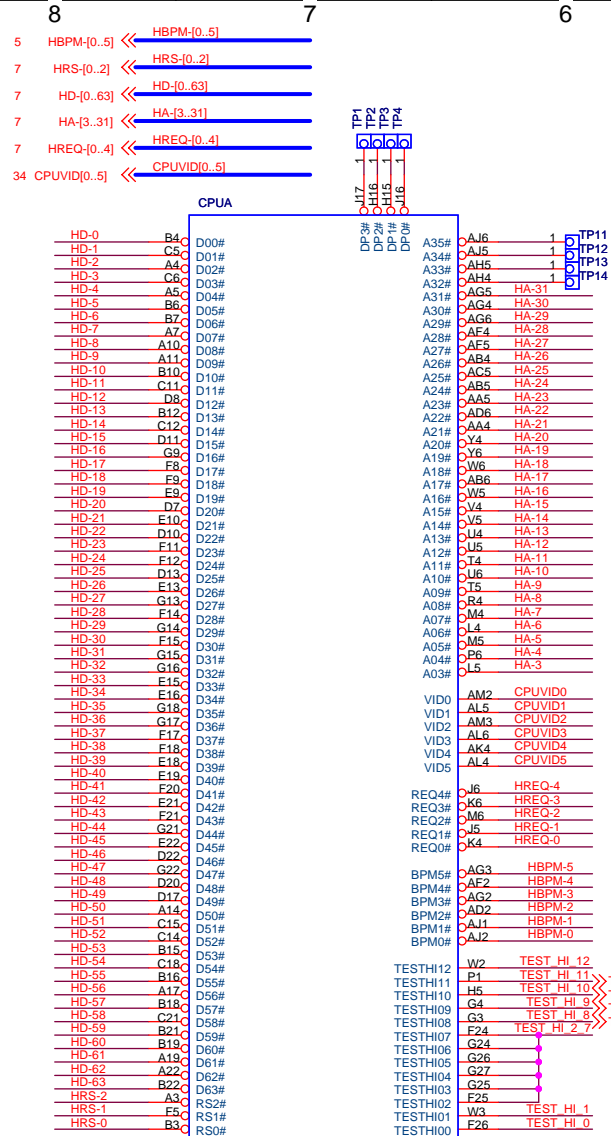
1. Page 5, modified R162 from 100 to 49.9.
2. Page 7, modified R126 from 14 to 10.
 - . Page 7, modified R117 from 100 to 120.
 - . Page 7, modified R756 from 619 to 261.
 - . Page 7, modified SR1 from 100 to 49.9.
 - . Page 7, modified SR4 from 169 to 100.
3. Page 15, modified R840, R841, and R842 from 1K to 4.7K.
 - and R843, R844, and R845 from 4.7K to 1K.
4. Page7, modified R804 from 124 to 150.
5. Page7, modified R805 from 500 to 680.
6. Page 34, modified PWM.
7. Page 8, R810 pull high to Vcc3.
 - . Page 12, modified R873, R874 from 1K to 4.7K.
9. Page 15, modified R73 from 22 to 33.
10. Page 15, modified C68 from 10p to 22p.
 - . Page 15, modified C101 from 10p to 22p.
11. Page 21, add U26-U29 four ESD IC.
 - . Page 21, add C1014 and C1016 for EMI.
12. Page 24, add D705-D708 four surge IC.
13. Page 26, add D703 and D704 for preventing pop noise.
14. Page 27, add C1018, C1019, and C1020 for EMI.
15. Page 27, add C1012(1U) to solve MIC issue.
16. Page 27, fine tune audio interface resistance and capacitance.
17. Page 28, changed ITE 8705 to ITE 8712.
18. Page 32, modified R288 from 200 to 187.
19. Page 33, use Q7 and Q8 to replace Vcc_Dual circuit.
20. Page 5, modified to support Smithfield.

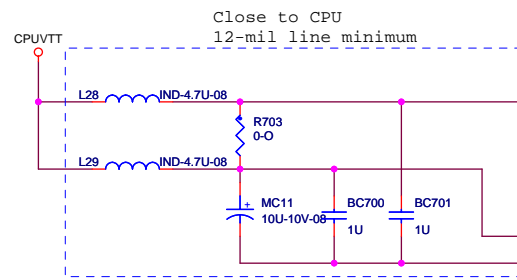
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DESIGNER	<i>LukeLin</i>	
LAYOUT	<i>ECS Layout team</i>	
CHECK	<i>LukeLin</i>	
APPROVAL		

 Elitegroup Computer Systems		
Title 649-M3		
Size	Document Number	Rev
Custom	<i>Cover Sheet</i>	1.0
Date: <i>Wednesday, June 15, 2005</i> Sheet <i>1</i> of <i>36</i>		

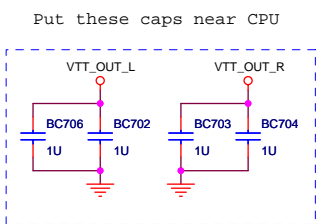
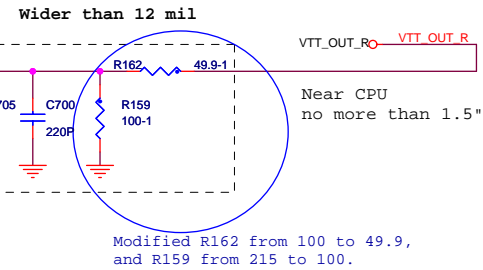
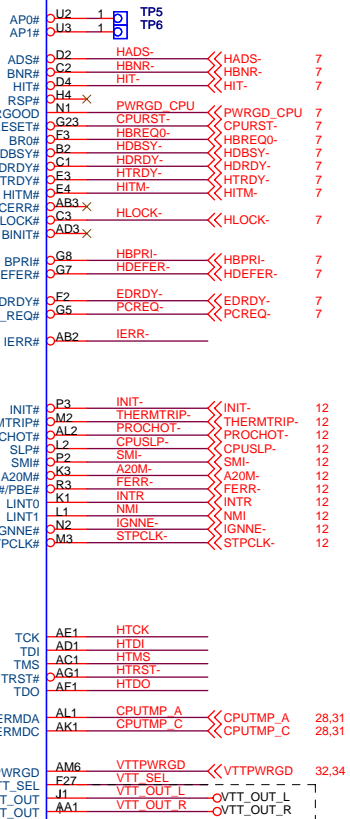
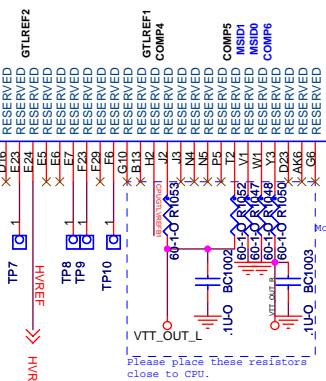
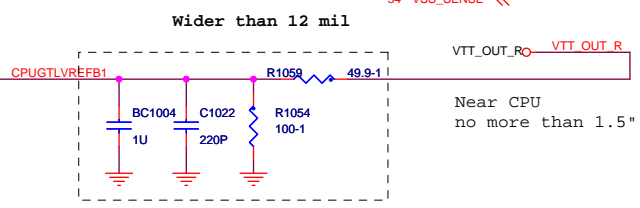
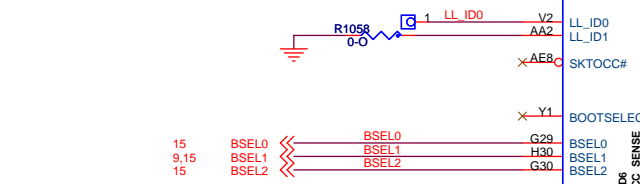
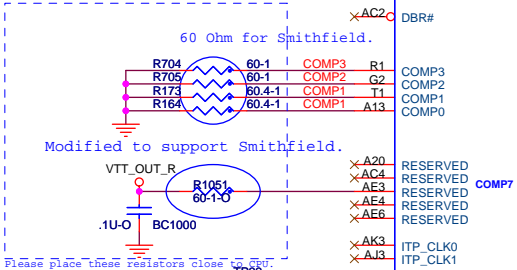
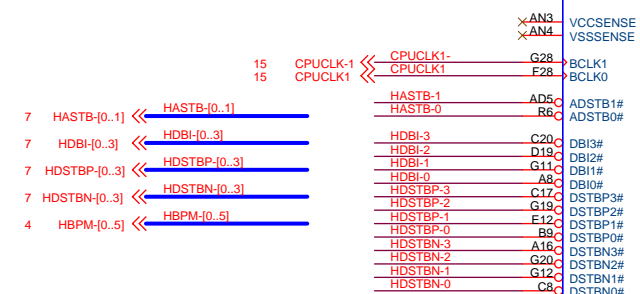




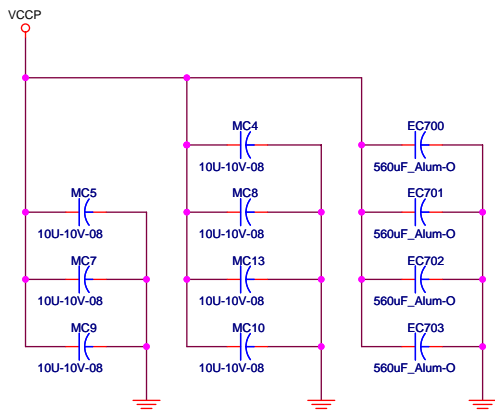




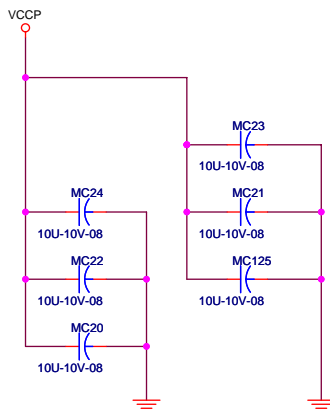
P4PEE
L : RESET#, BR0#, PWRGD, TESTHI1,8,9,10,11,12 = VCCP
R : VITPWRGD, VID[5:0], GTLREF, TMS, TDI, TDO, BPM[5:0], VREG = VTT_OUT



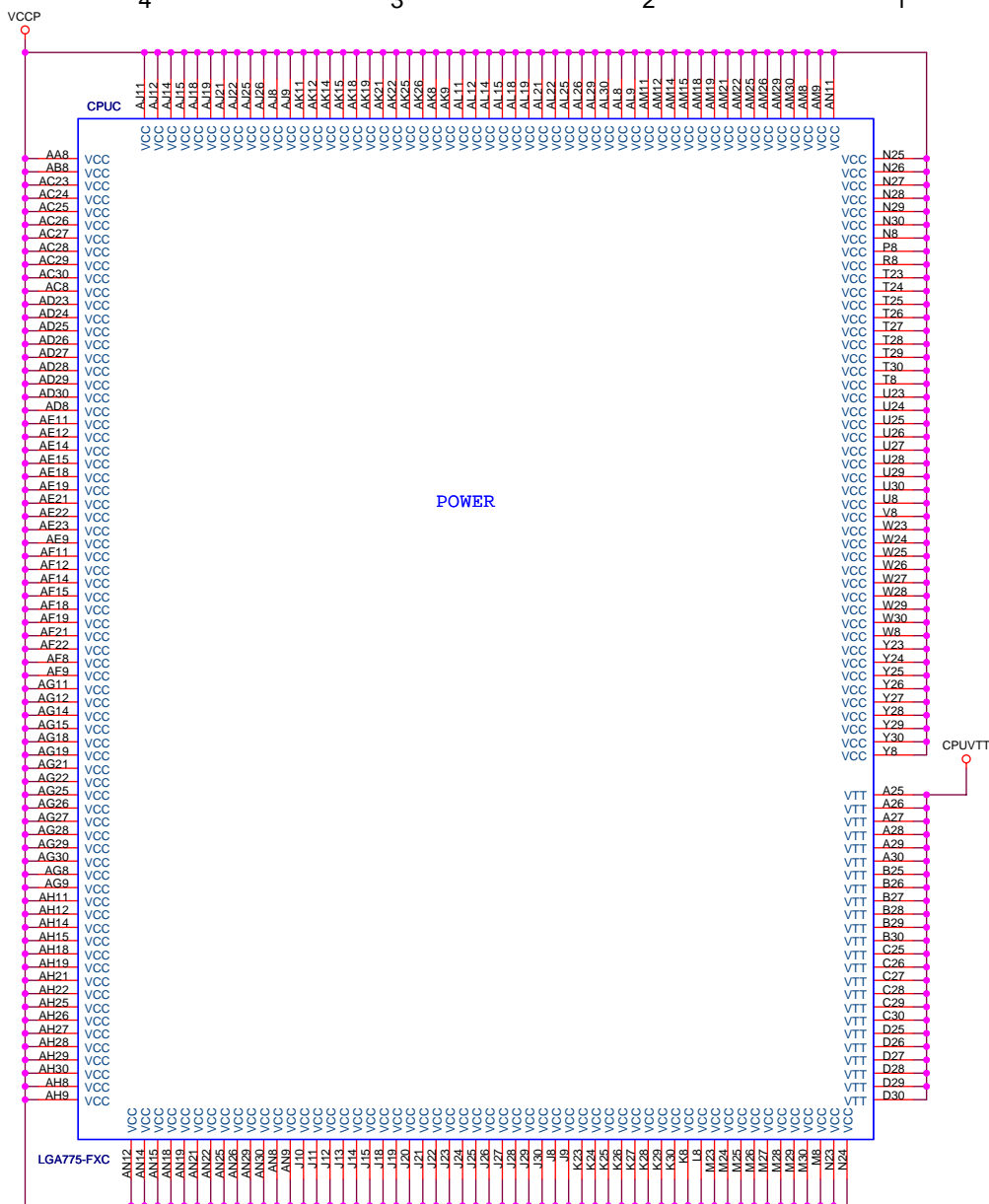
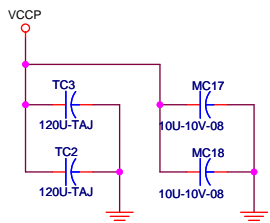
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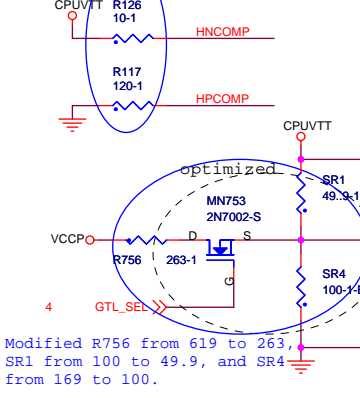
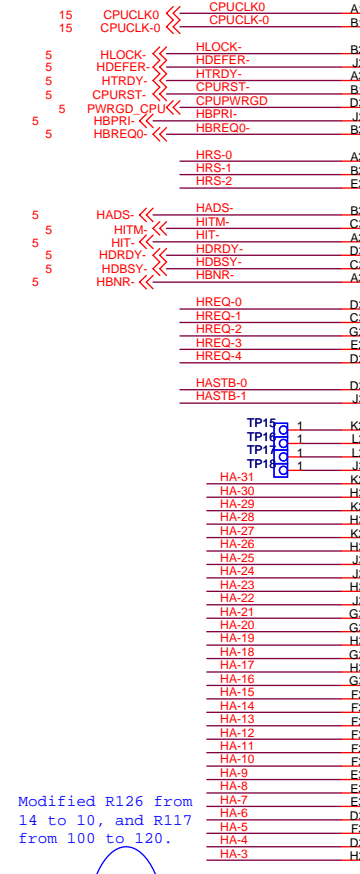
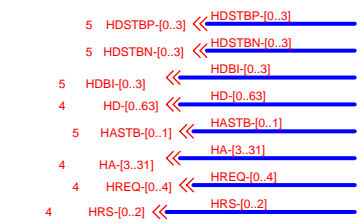


Put these capacitors at processor LEFT SIDE

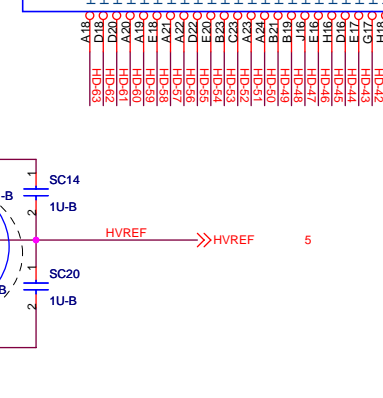
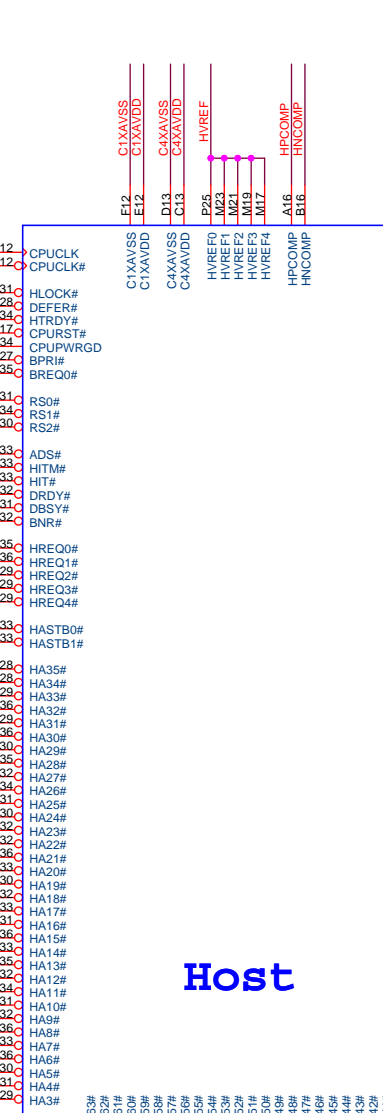


Put these capacitors INSIDE PROCESSOR CAVITY

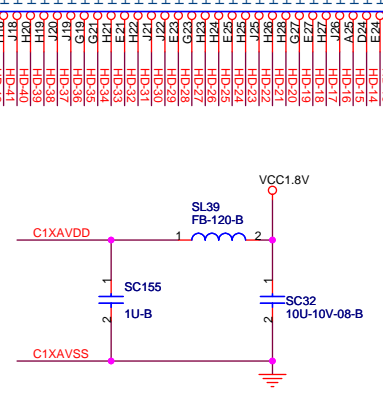
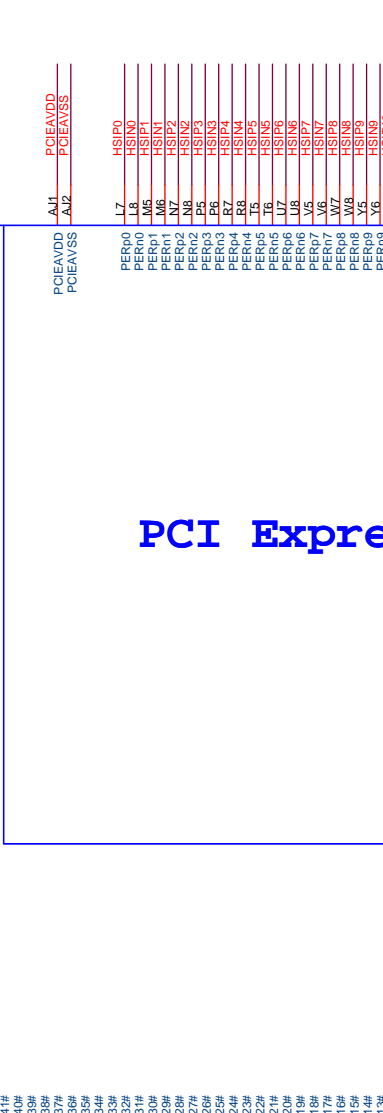




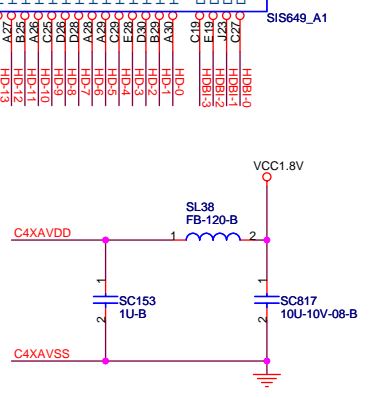
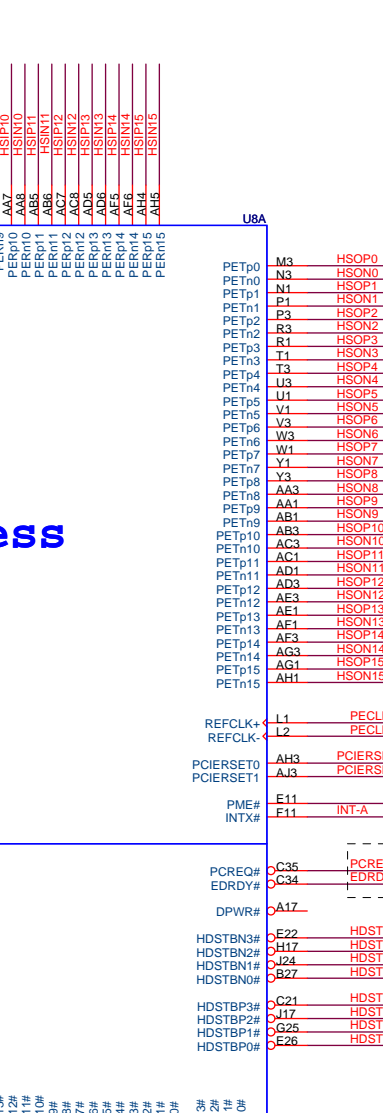
Modified R126 from 14 to 10, and R117 from 100 to 120.



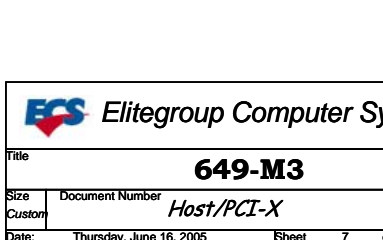
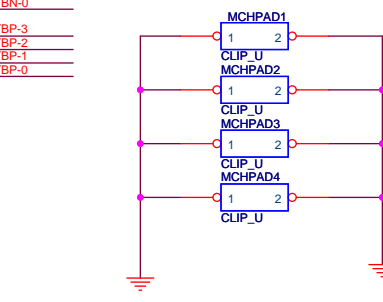
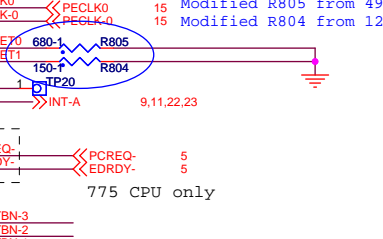
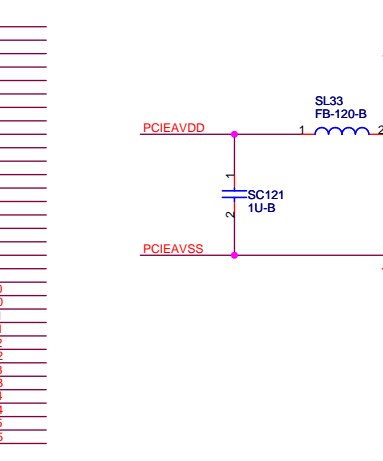
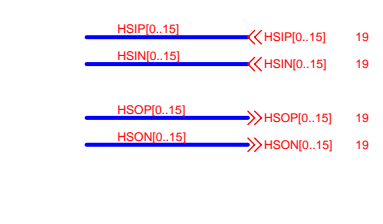
Modified R756 from 619 to 263, SR1 from 100 to 49.9, and SR4 from 169 to 100.



Modified R756 from 619 to 263, SR1 from 100 to 49.9, and SR4 from 169 to 100.




Modified R756 from 619 to 263, SR1 from 100 to 49.9, and SR4 from 169 to 100.



Modified R805 from 499 to 680, and R804 from 124 to 150.

PCI Express

Host



Elitegroup Computer Systems

649-M3

Host/PCI-X

Title

Size

Custom

Date

Document Number

Thursday, June 16, 2005

Rev

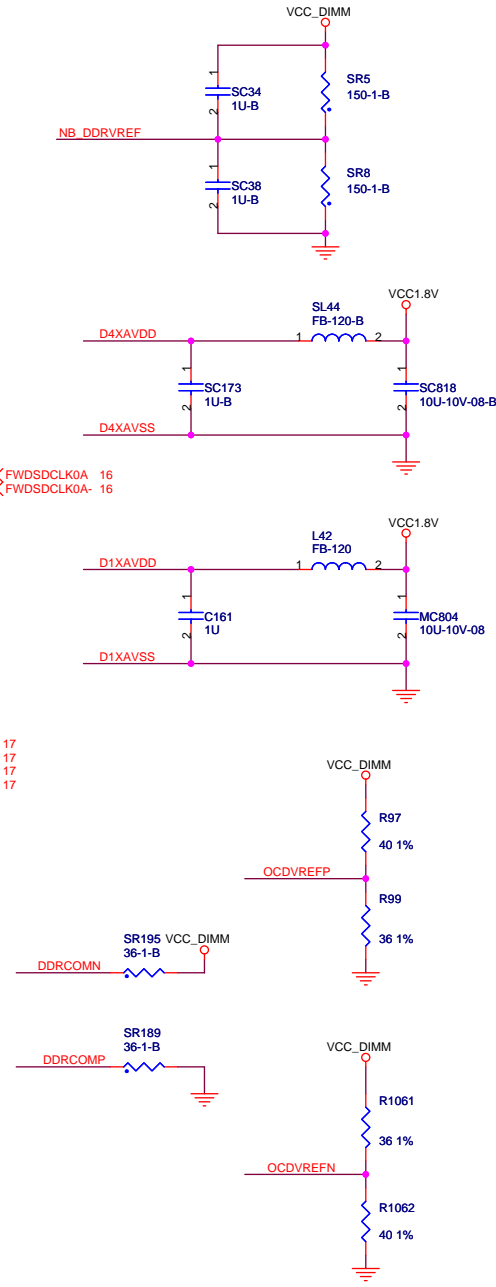
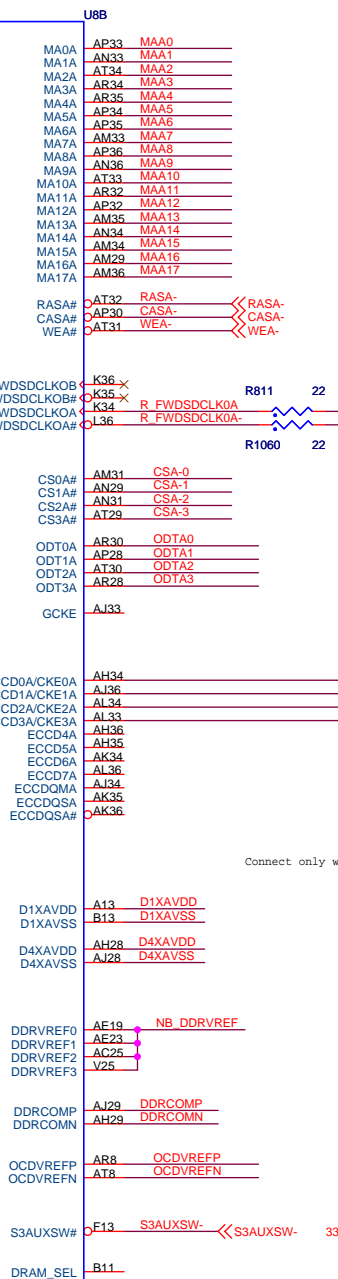
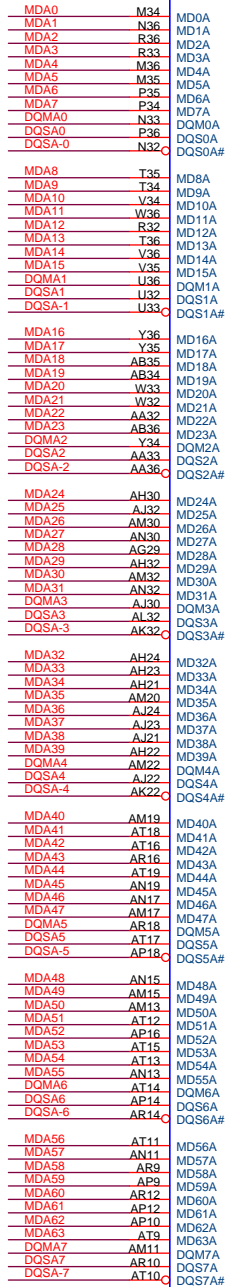
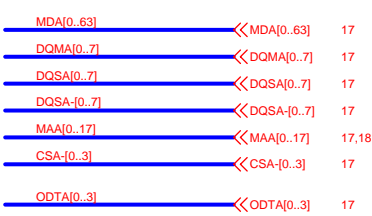
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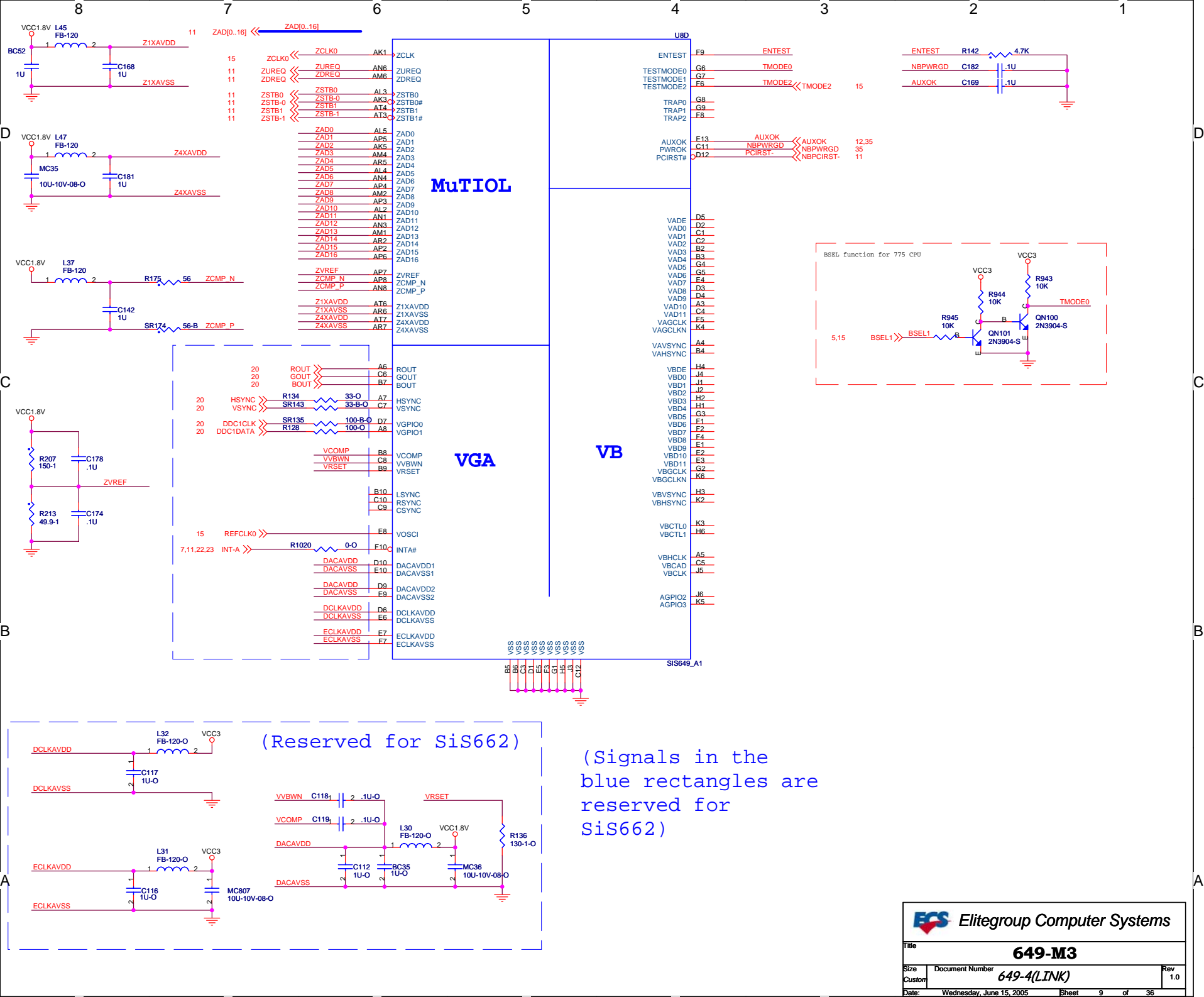
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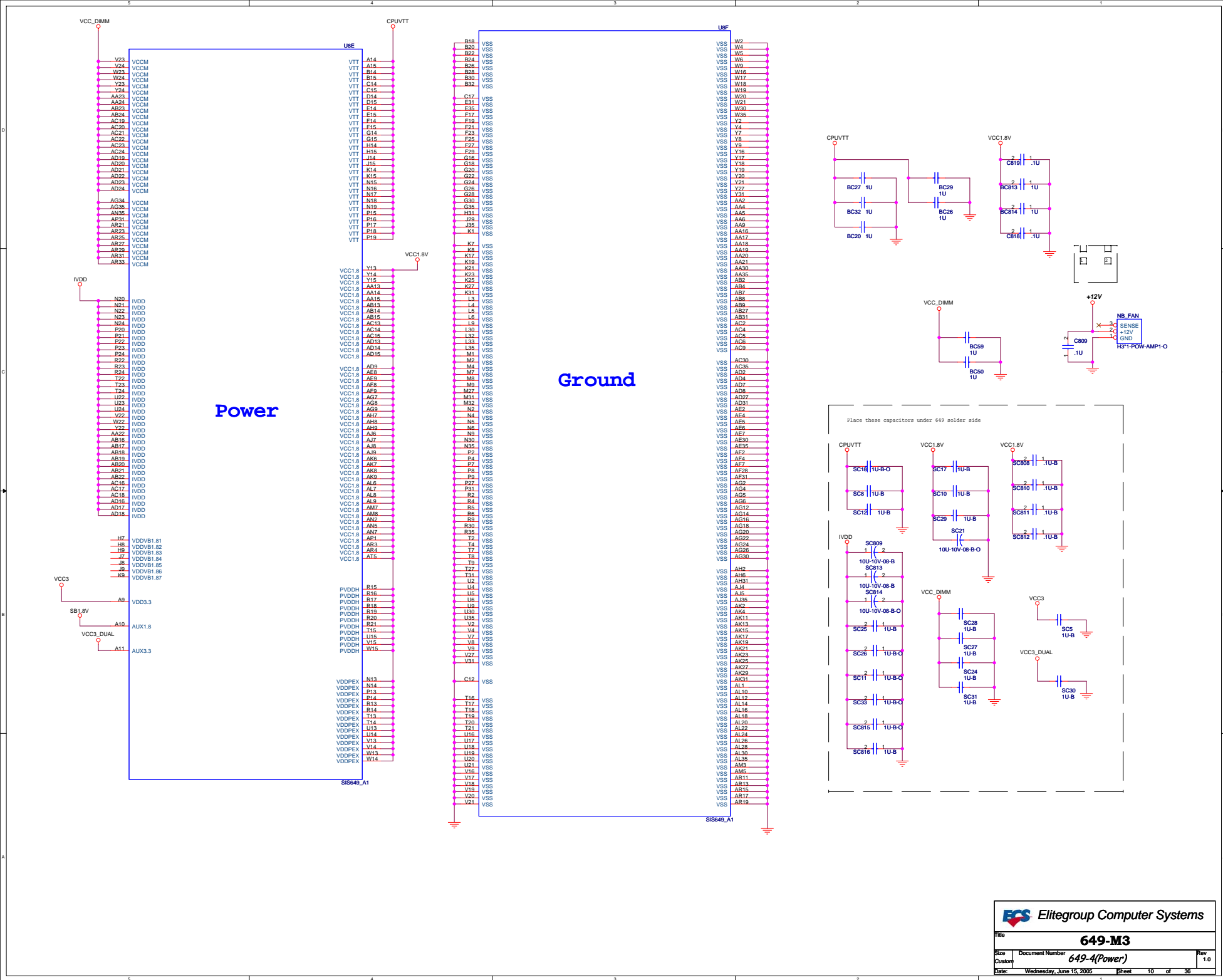
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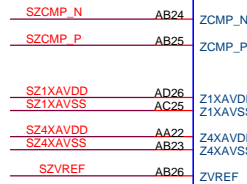
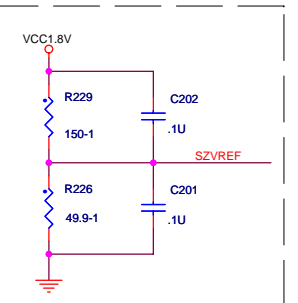
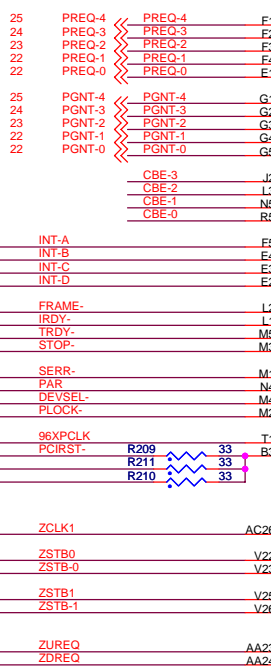
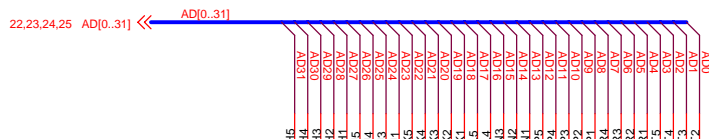
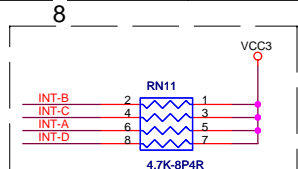
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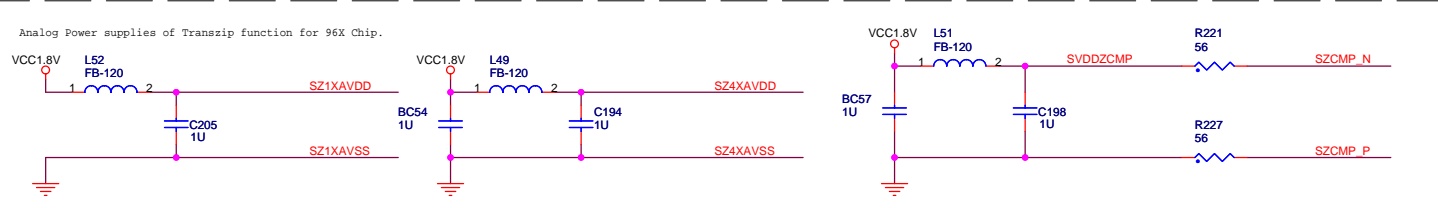
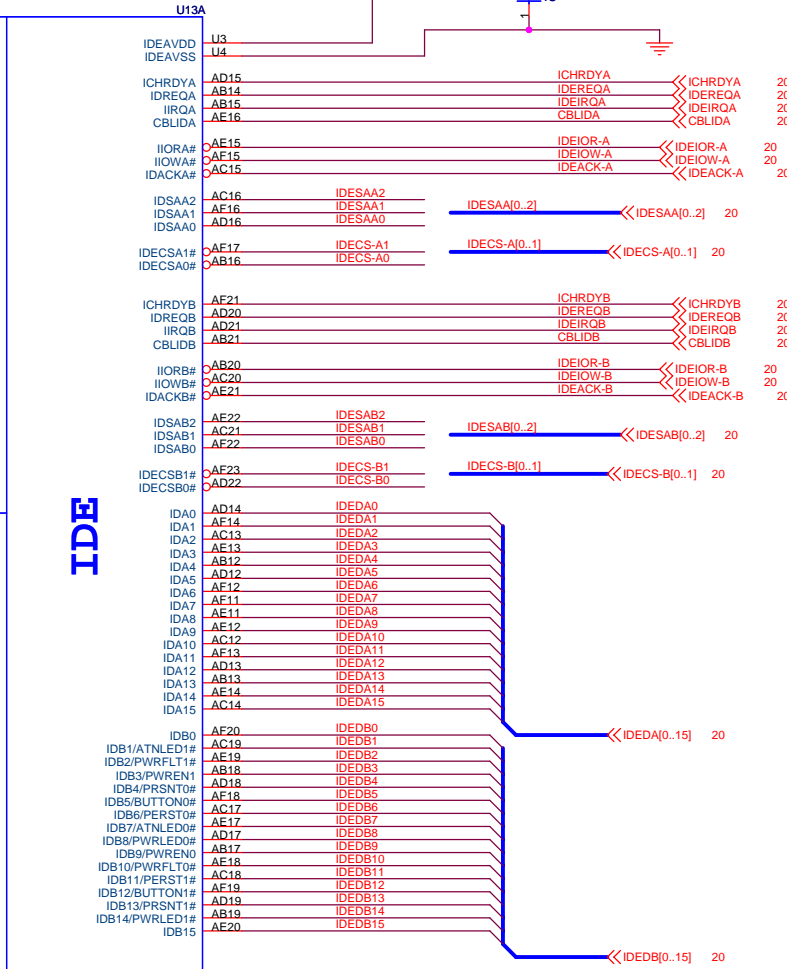


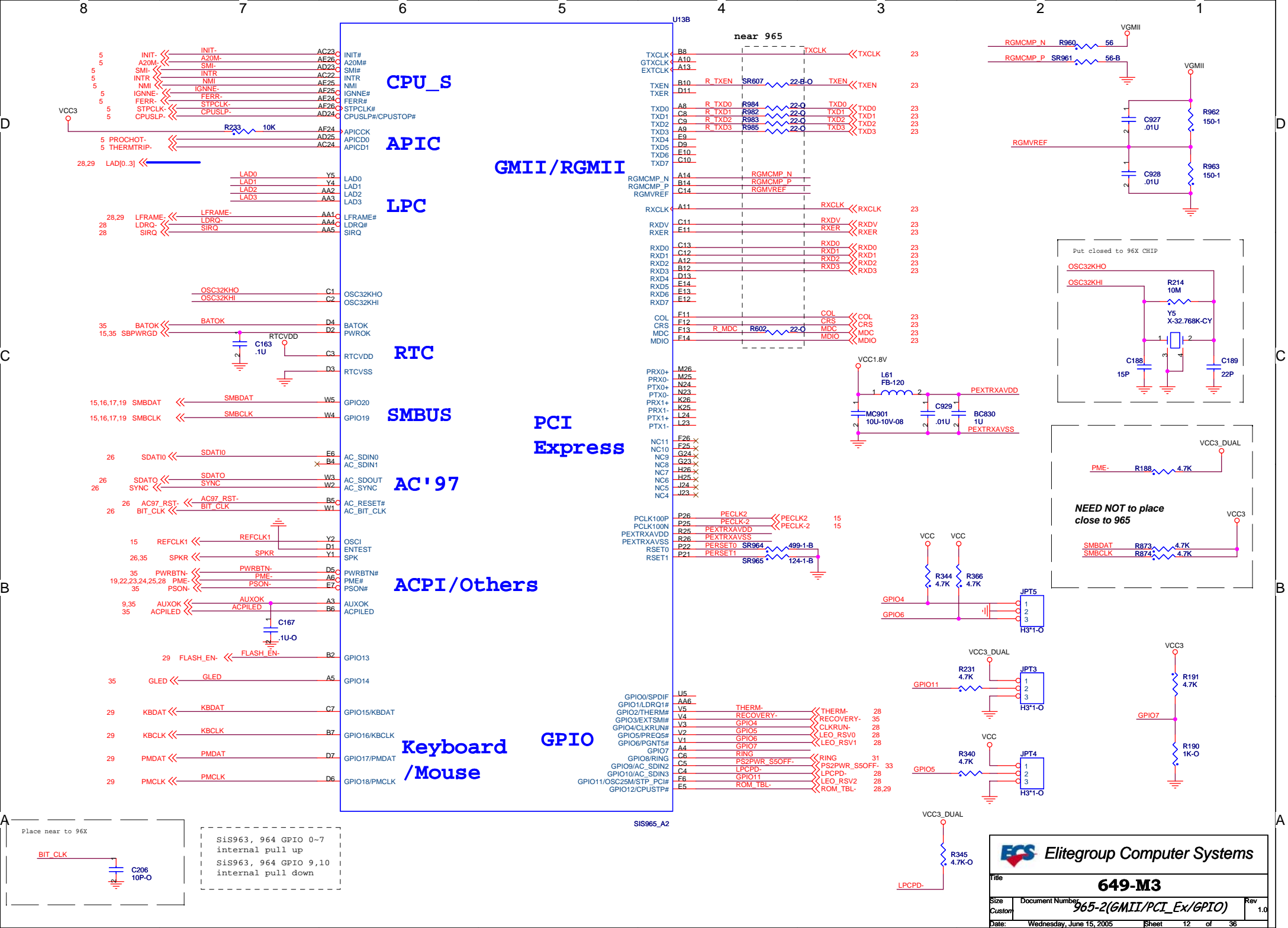


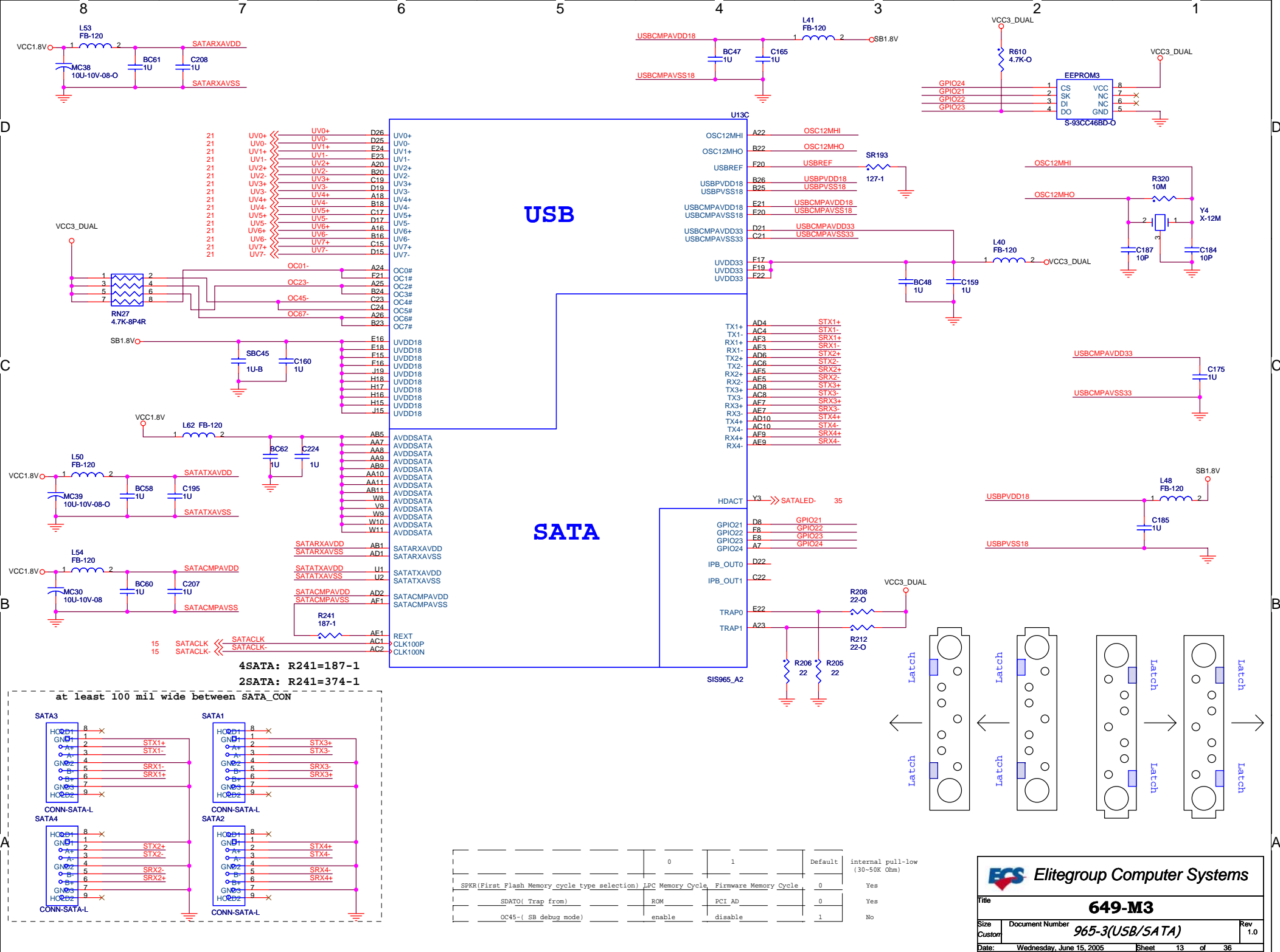
PCI

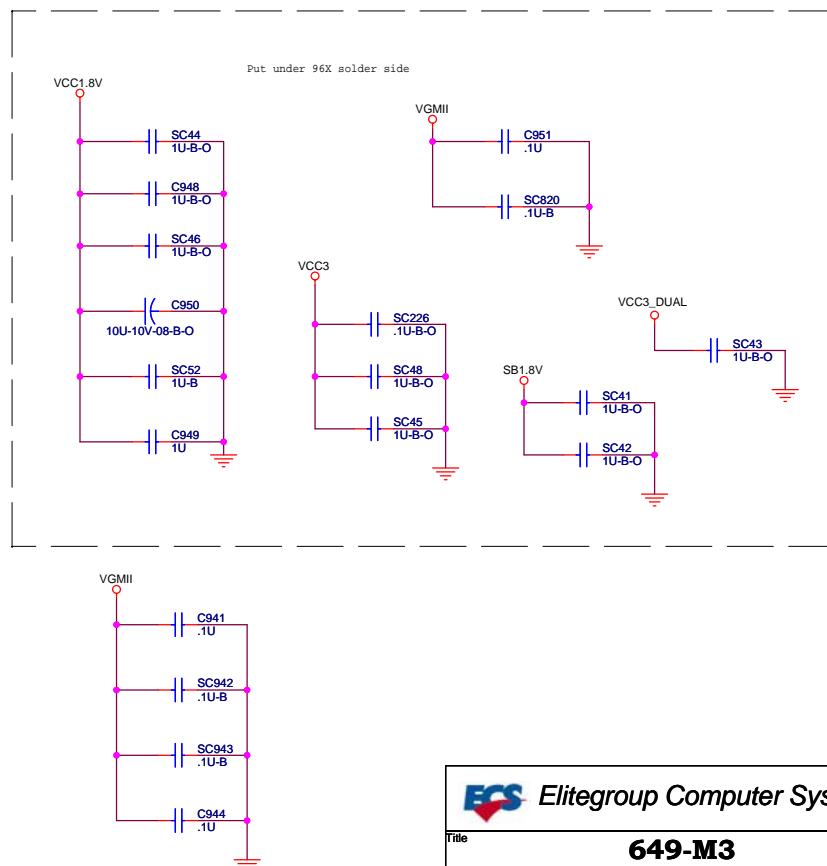
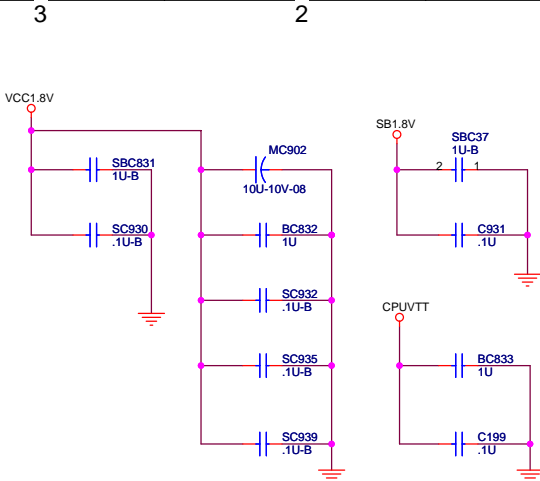
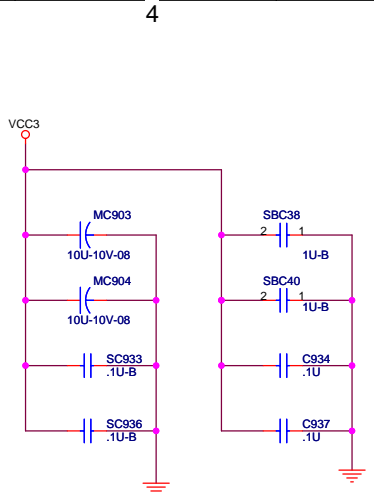
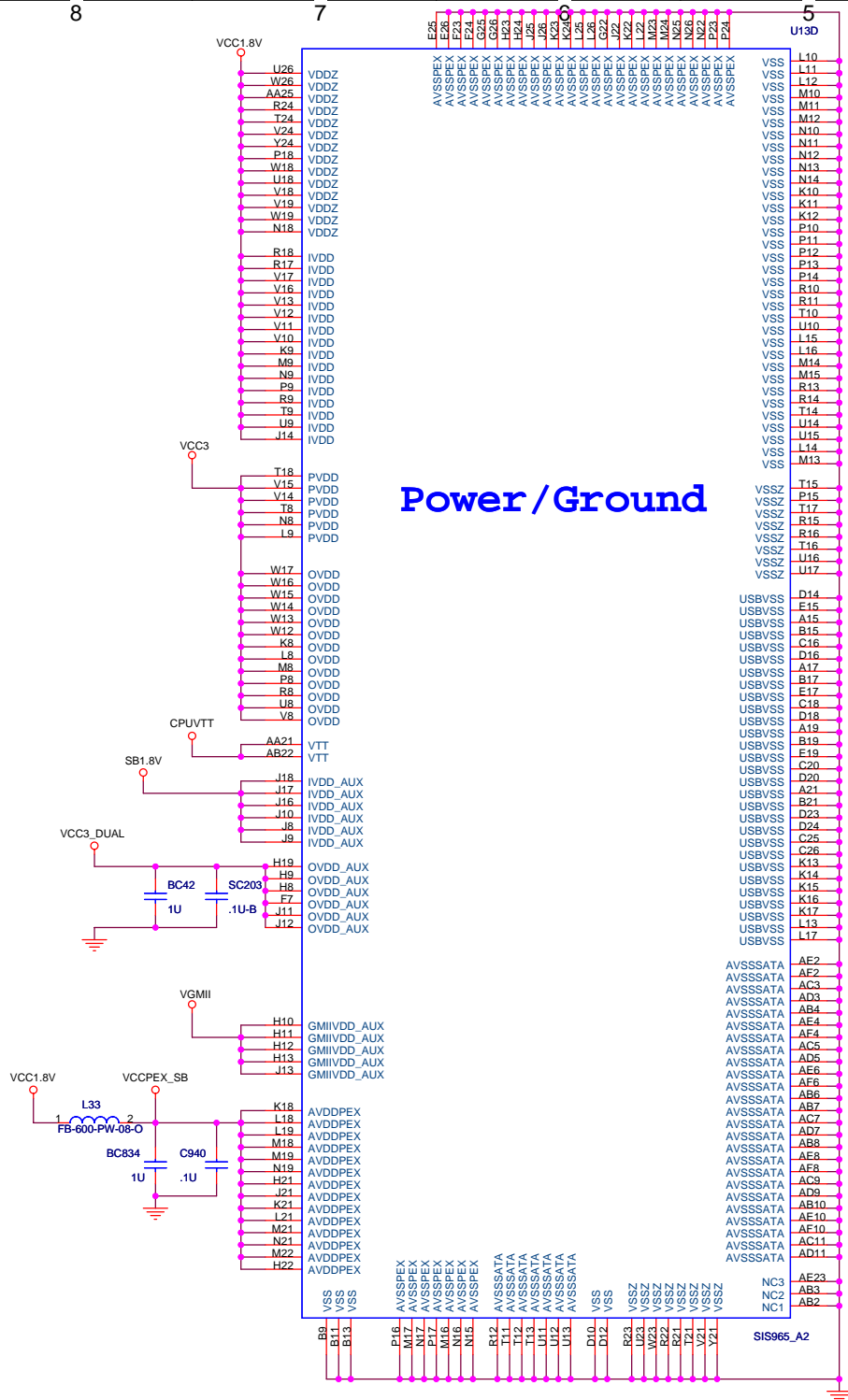
MuTIOL

IDE

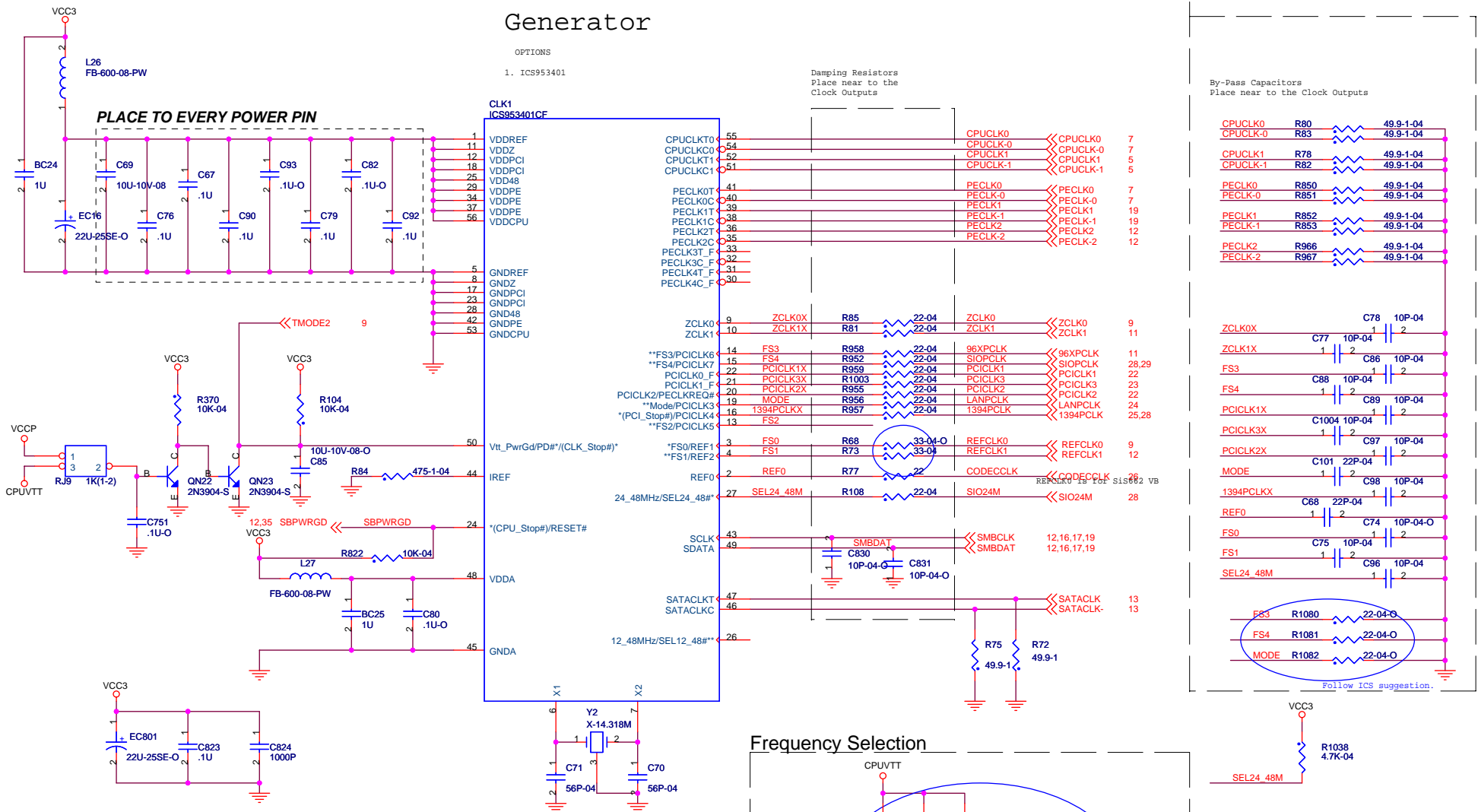






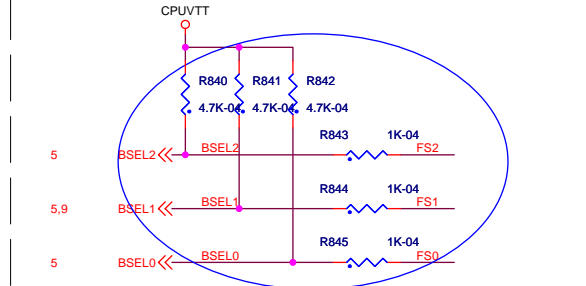


Main Clock Generator



Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	Low	BSEL2	BSEL1	BSEL0
CPU=100 (BSEL[2:0]=101)	0	0	1	0	1
CPU=133 (BSEL[2:0]=001)	0	0	0	0	1
CPU=166 (BSEL[2:0]=011)	0	0	0	1	1
CPU=200 (BSEL[2:0]=010)	0	0	0	1	0
CPU=266 (BSEL[2:0]=000)	0	0	0	0	0
CPU=333 (BSEL[2:0]=100)	0	0	1	0	0
CPU=400 (BSEL[2:0]=110)	0	0	1	1	0

Frequency Selection

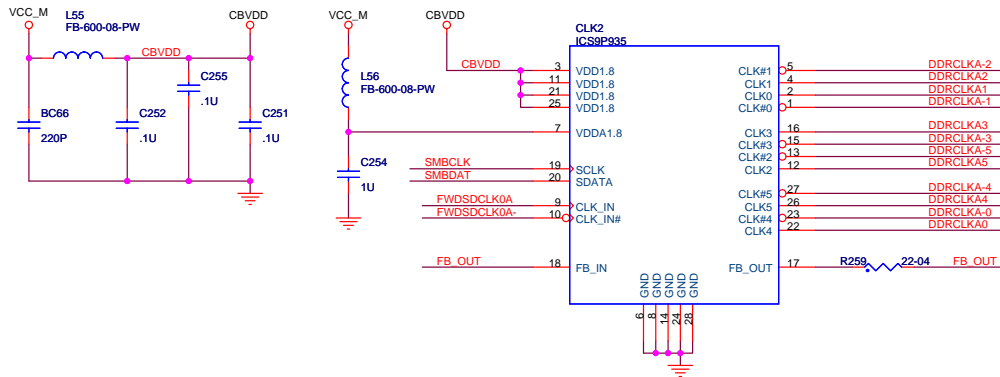


Modified R840, R841, and R842 from 1K to 4.7K, and R843, R844, and R845 from 4.7K to 1K.

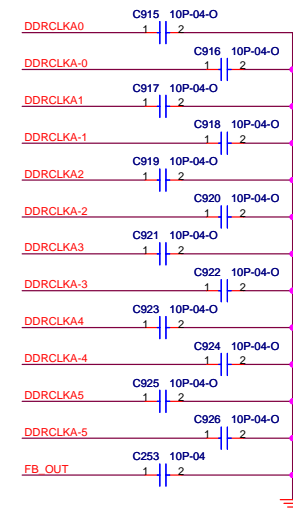
Clock Buffer (DDRII)

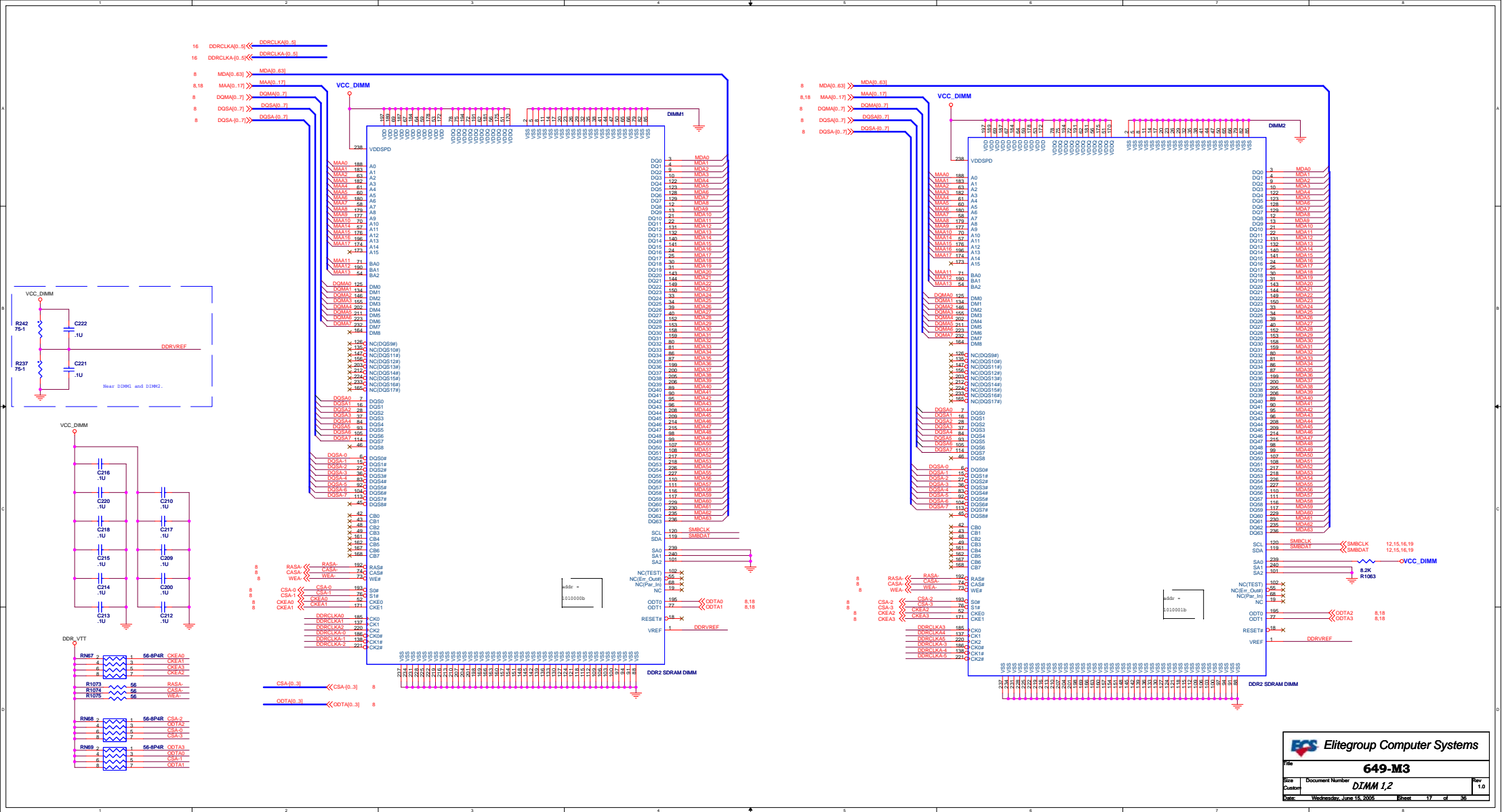
(5 OPTIONS)
 1:: (ICS) ICS93716
 2:: (Winbond)
 3:: (ICWorks)
 4:: (IMI)
 5:: (AMI)

By-Pass Capacitors
 Place near to the Clock Buffer



DDRCLKA[0..5] << DDRCLKA[0..5] 17
 DDRCLKA[0..5] << DDRCLKA[0..5] 17
 SMBCLK << SMBCLK 12,15,17,19
 SMBDAT << SMBDAT 12,15,17,19
 FWSDCLK0A << FWSDCLK0A 8
 FWSDCLK0A- << FWSDCLK0A- 8

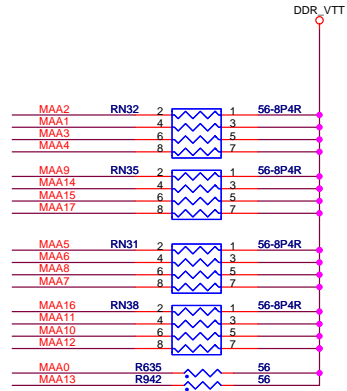




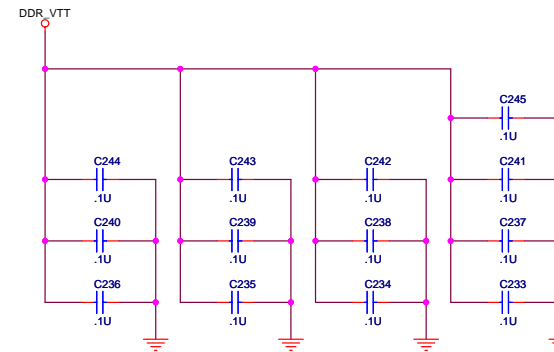
SSTL-2 Termination Resistors

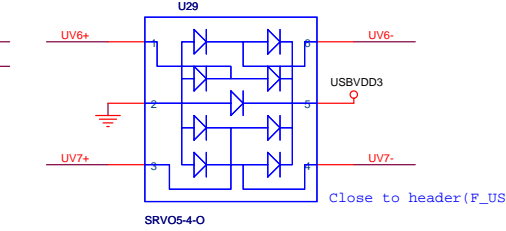
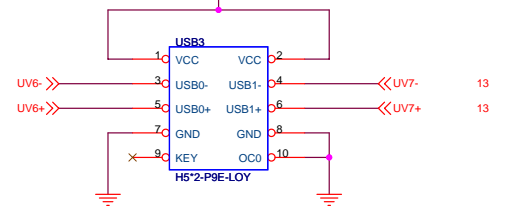
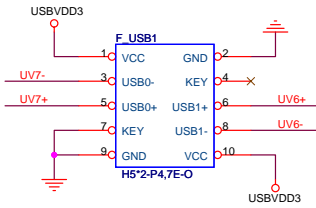
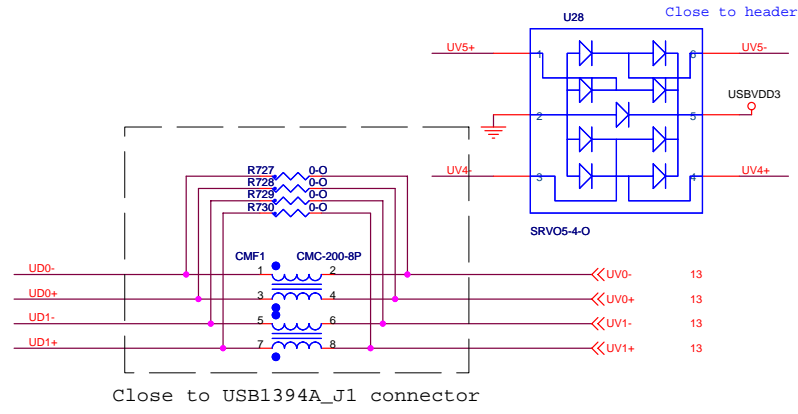
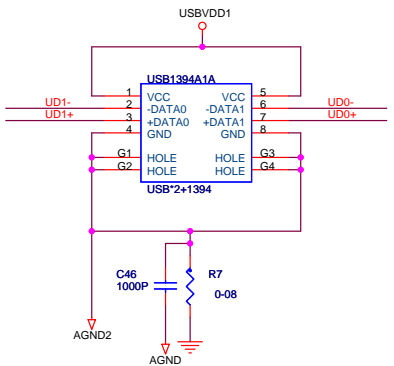
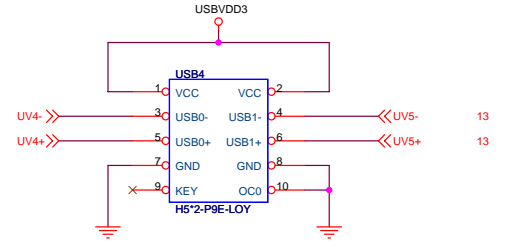
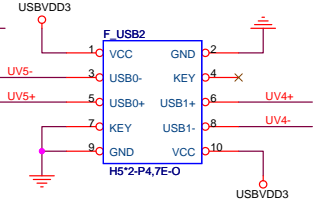
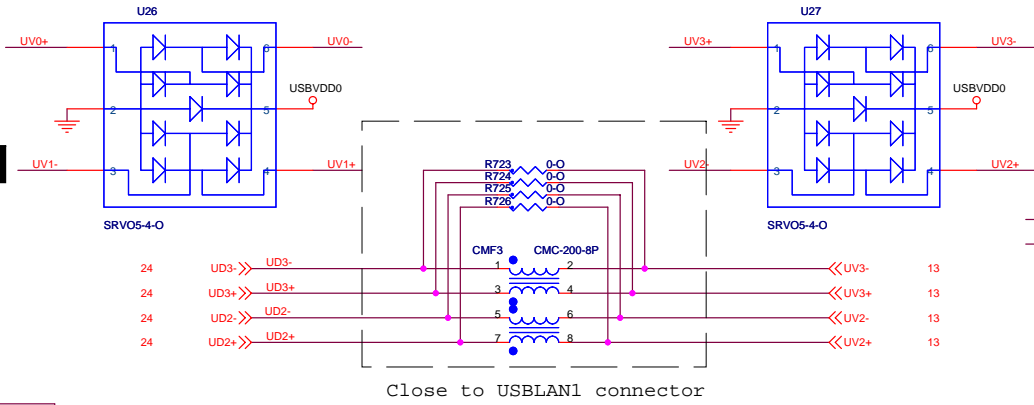
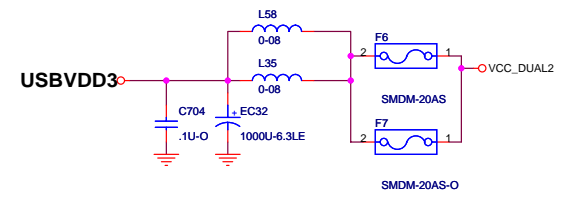
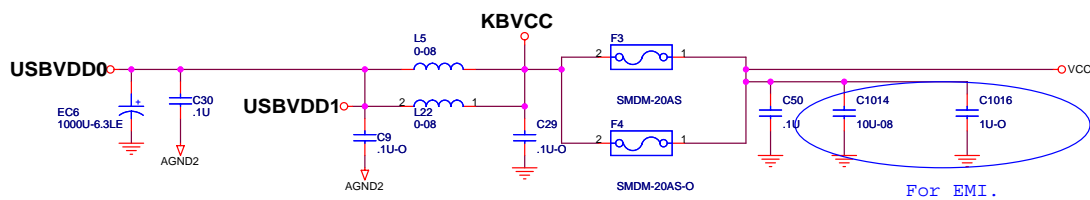
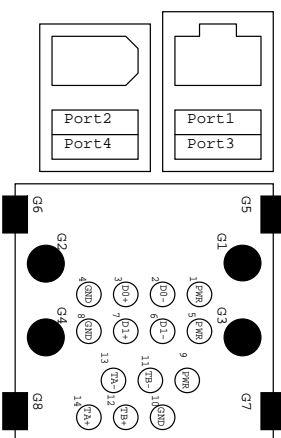
	SDR		DDR		
MD/DQM(/DQS)	LV-CMOS	Ra	SSTL-2	Ra	Rtt
MA/Control	LV-CMOS	0/10/-	SSTL-2	1.0	33
CS	LV-CMOS	0	SSTL-2	0	33
CKE	DD 3.3V		DD 2.5V	0	47

MAA[0..17] <<MAA[0..17] 8,17

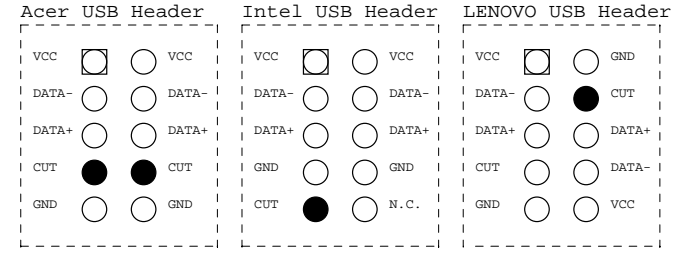
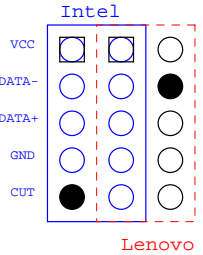
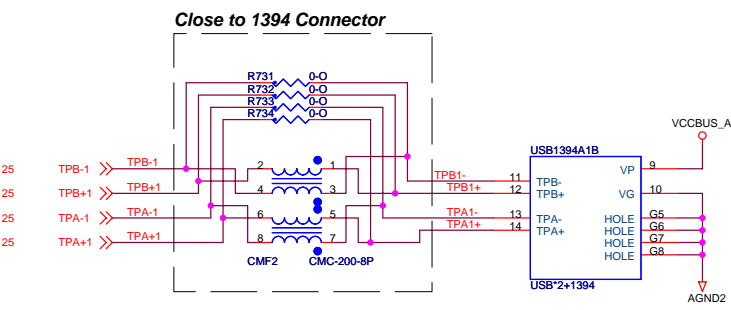
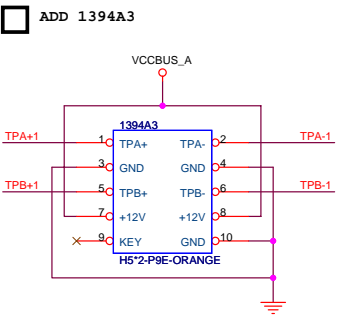


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
 0603 Package placed within 200mils of VTT Termination R-packs



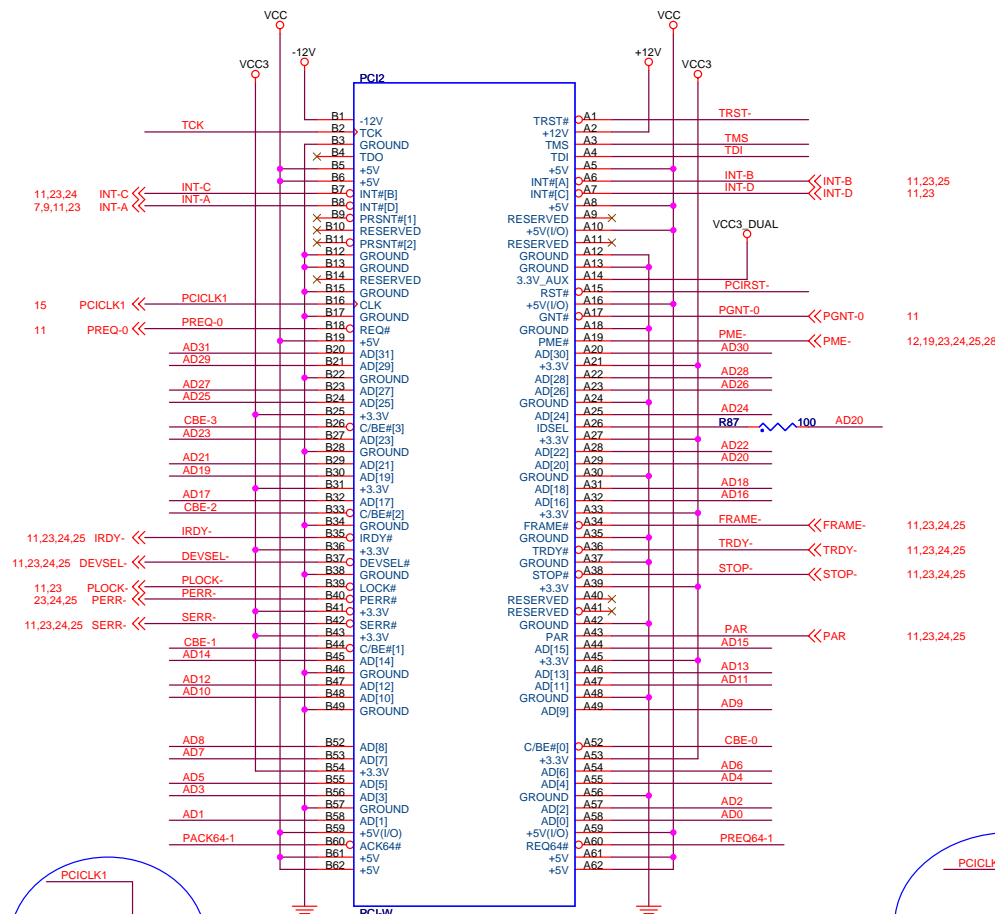


	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



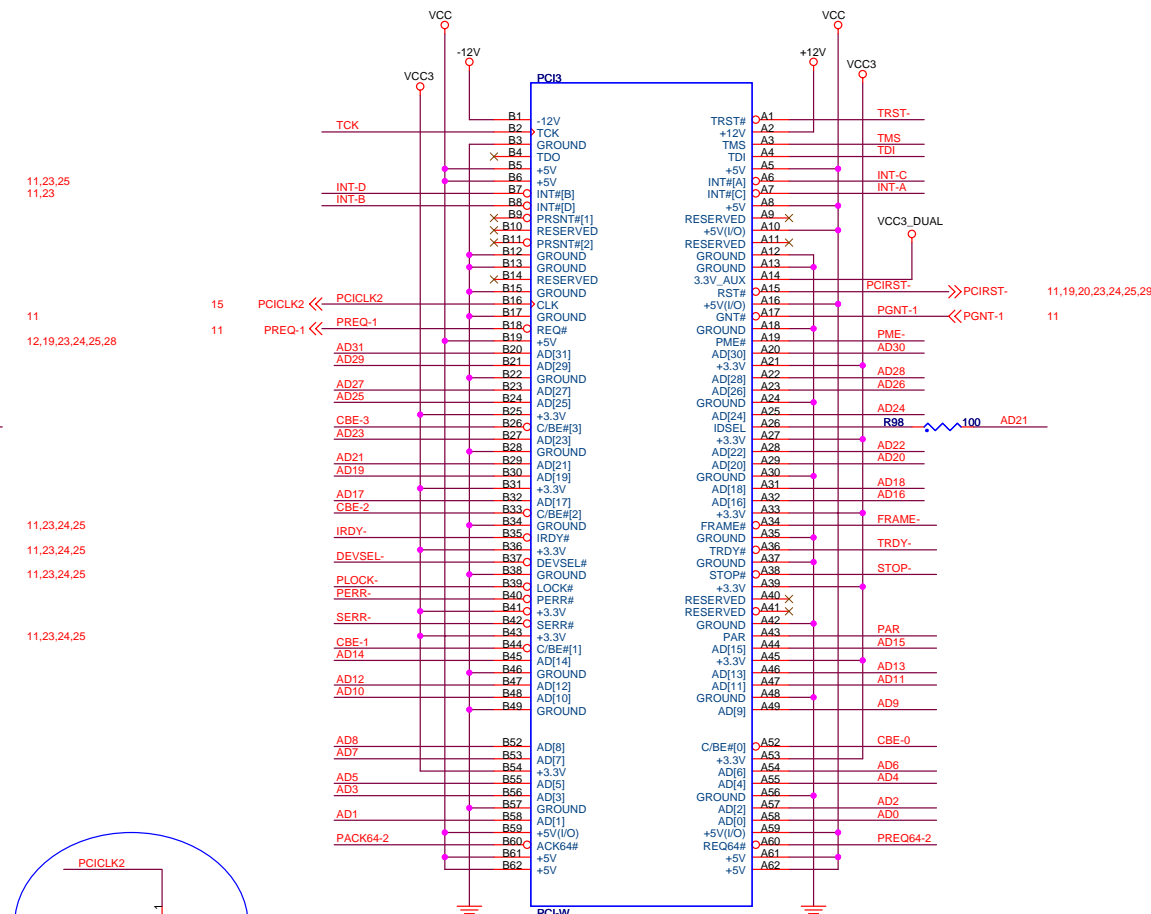
PCI Slot 1 & 2

11,23,24,25 CBE[0..3] << CBE[0..3]
11,23,24,25 AD[0..31] << AD[0..31]



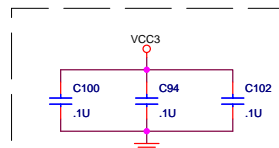
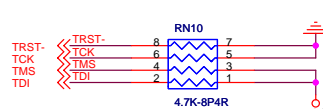
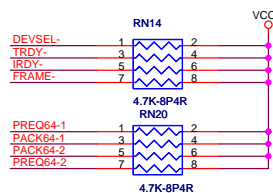
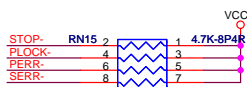
IDSEL=AD20
INT[B,C,D,A]
PCIx3=slot2
PCIEx1+PCIx2=slot1

Please place the cap close PCI Slot.

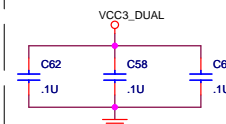


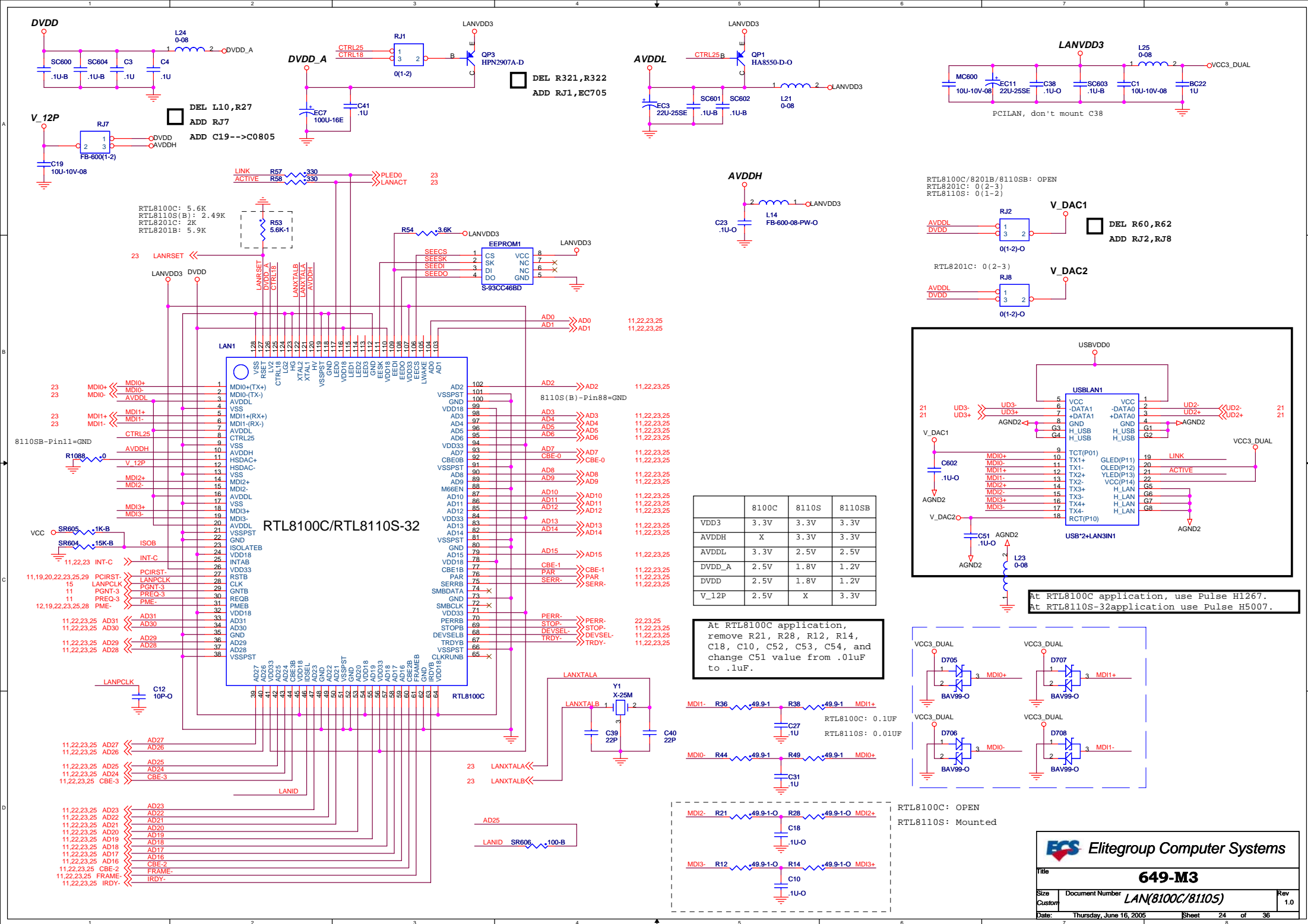
IDSEL=AD21
INT[C,D,A,B]
PCIx3=slot3
PCIEx1+PCIx2=slot2

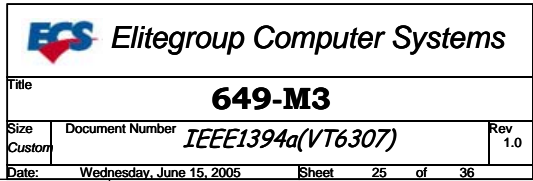
Please place the cap close PCI Slot.

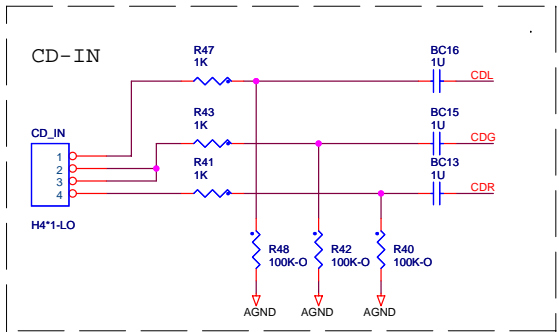


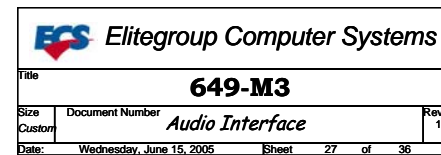
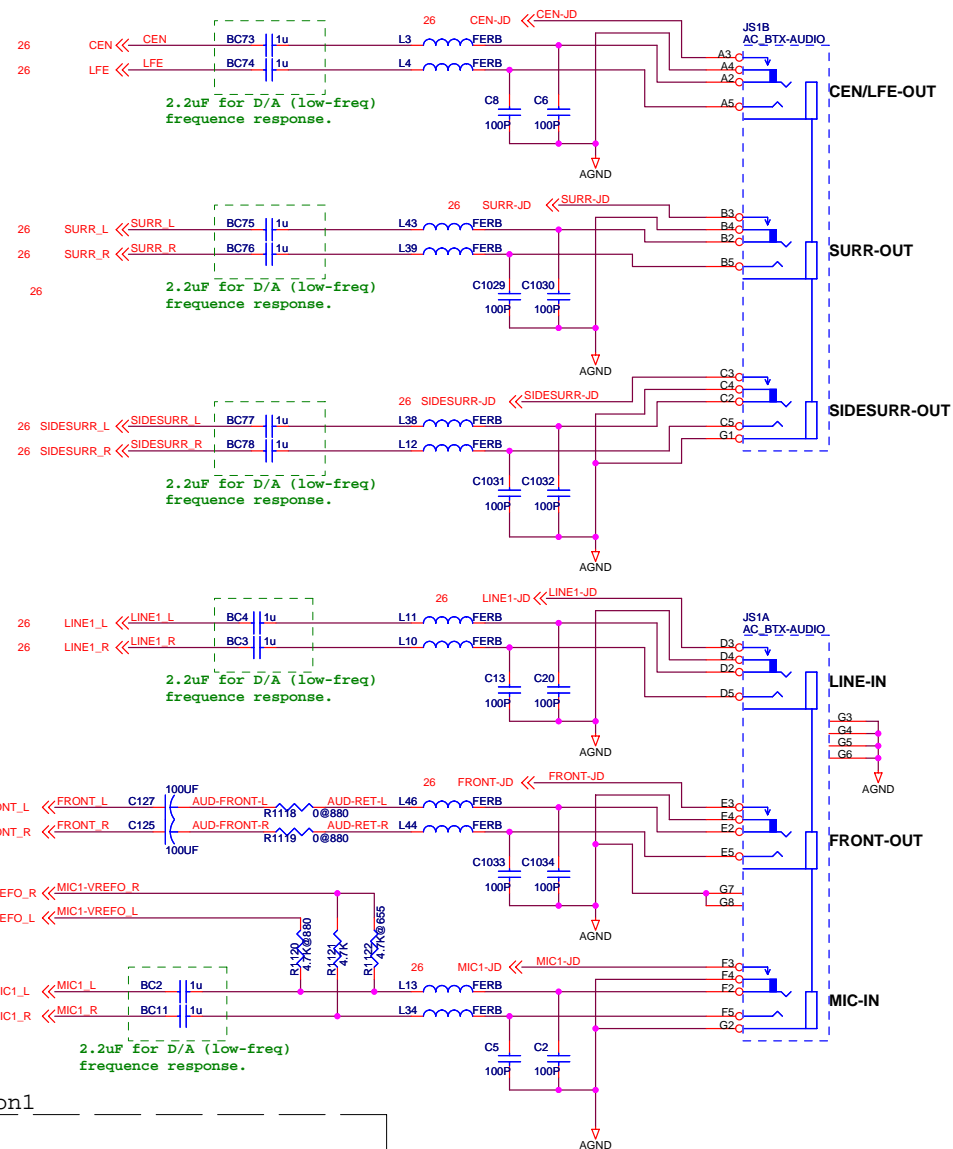
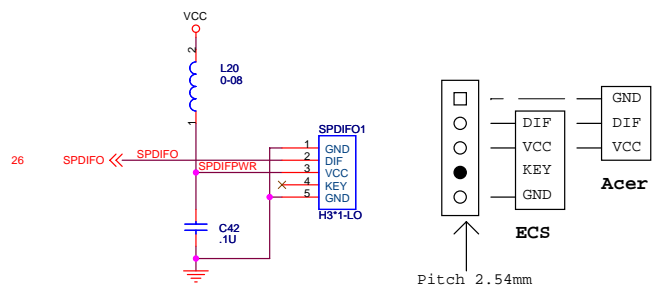
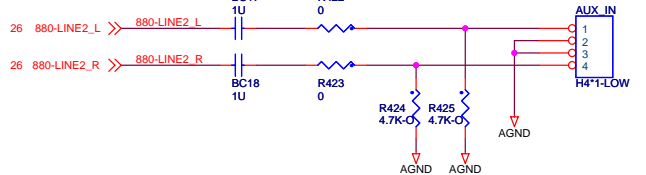
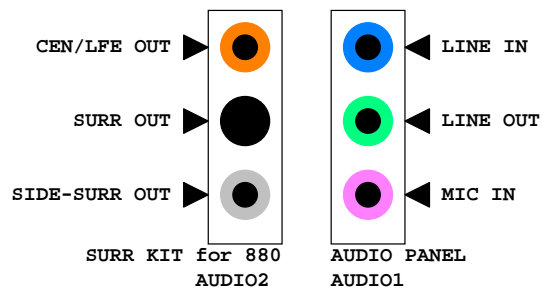
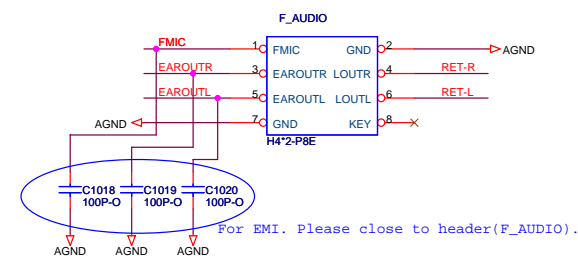
每個 PCI 插槽 pin A33
各放一顆

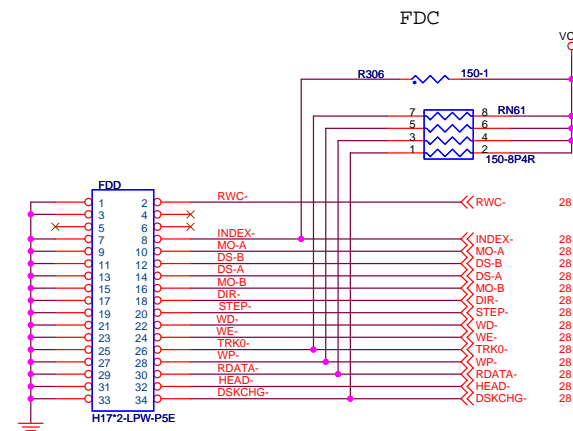
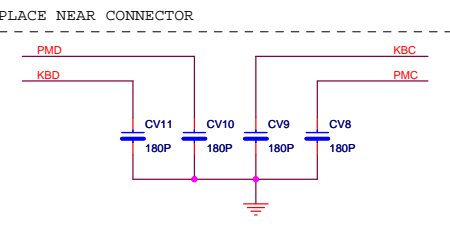
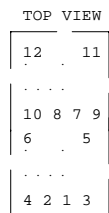








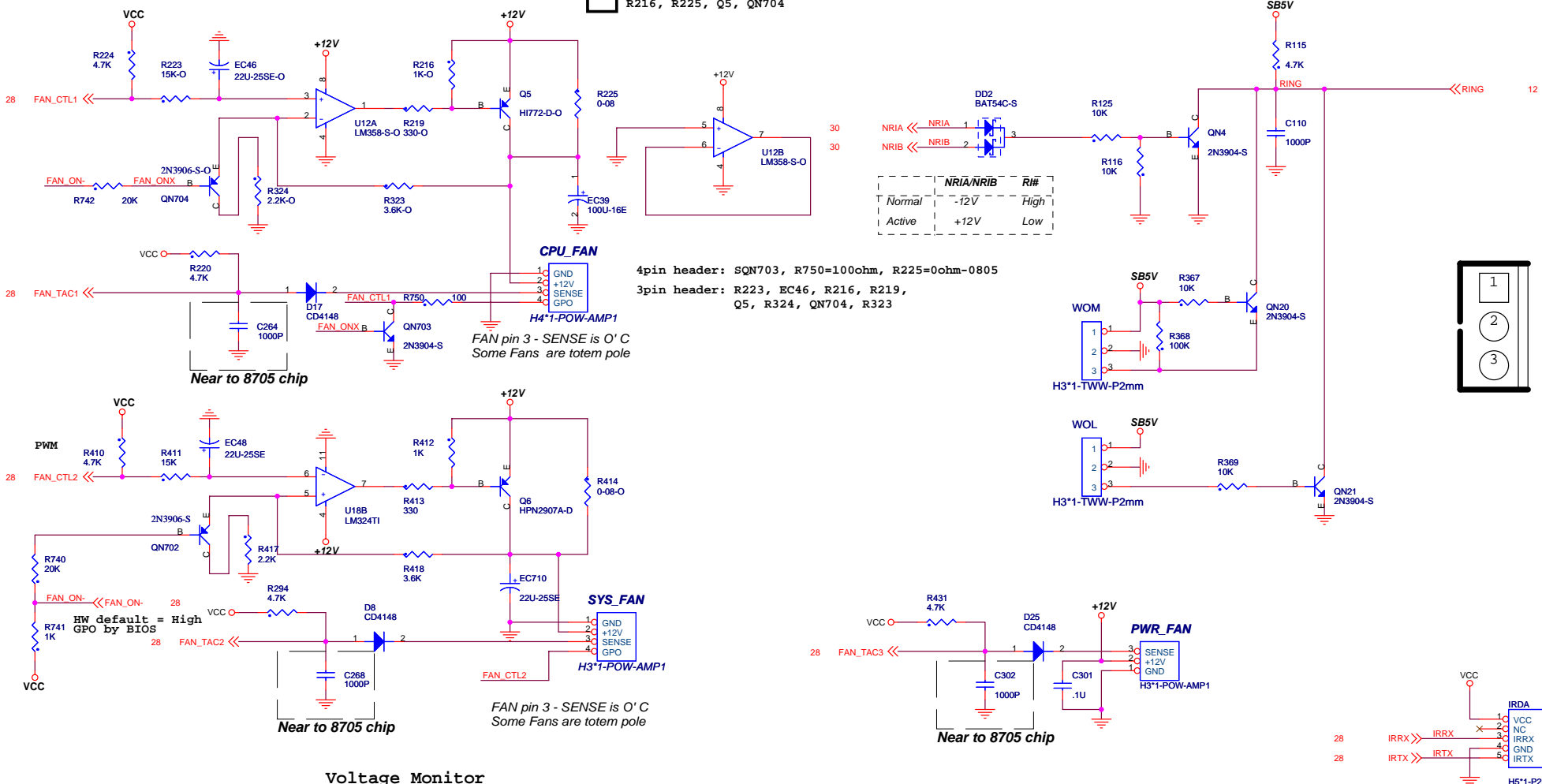




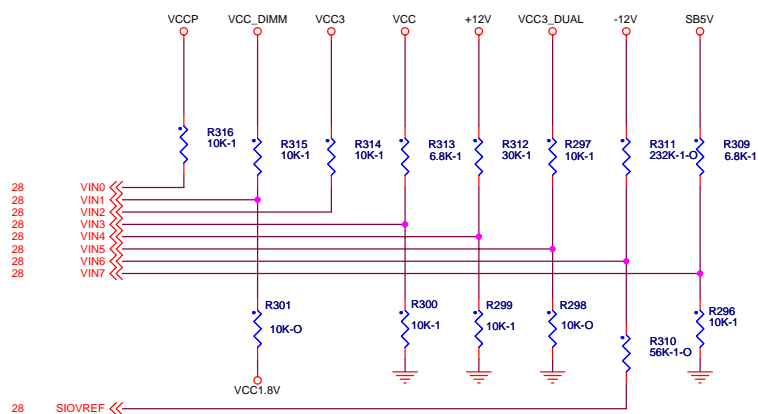
Layout:

Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

ADD R223, EC46, R323, R324, R219, R216, R225, Q5, QN704

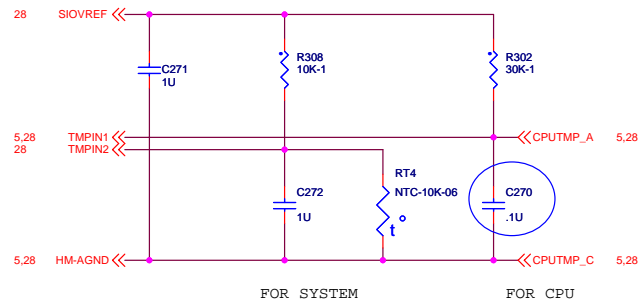


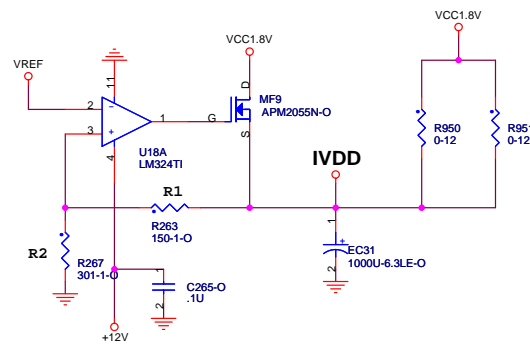
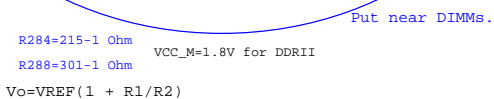
Voltage Monitor



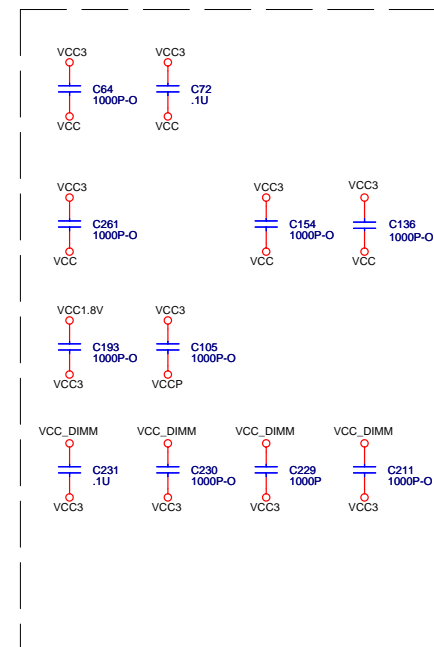
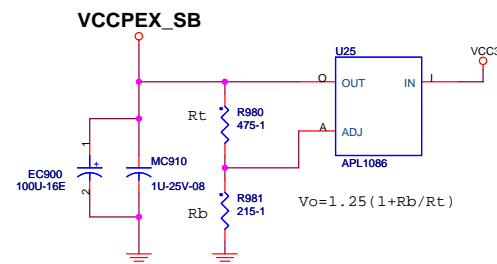
Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode





$VCC1.5V$ Max Power = $0.3*(0.289+2.35)=0.7917W$



平均分佈在POWER PLAN 和 PLAN 之間

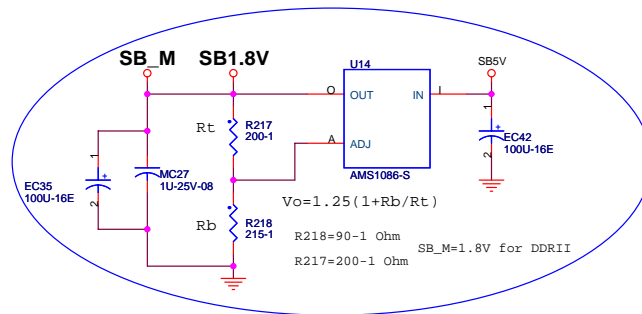
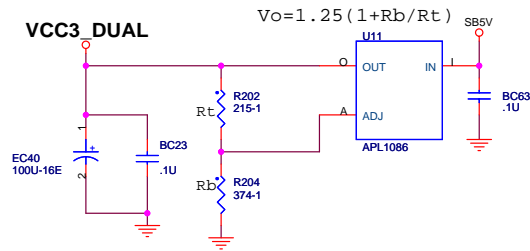
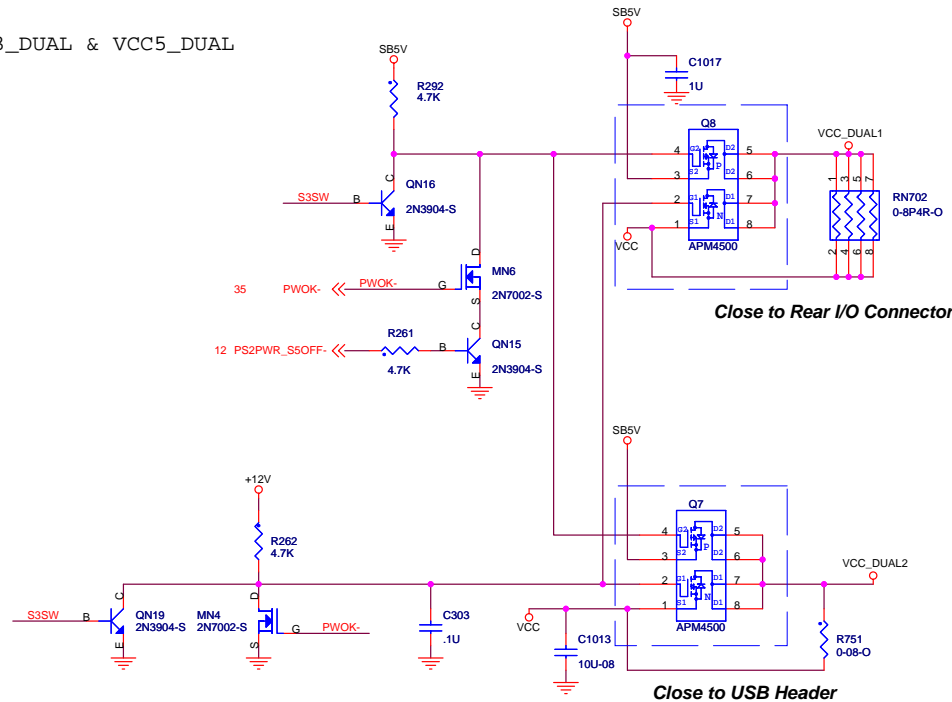
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

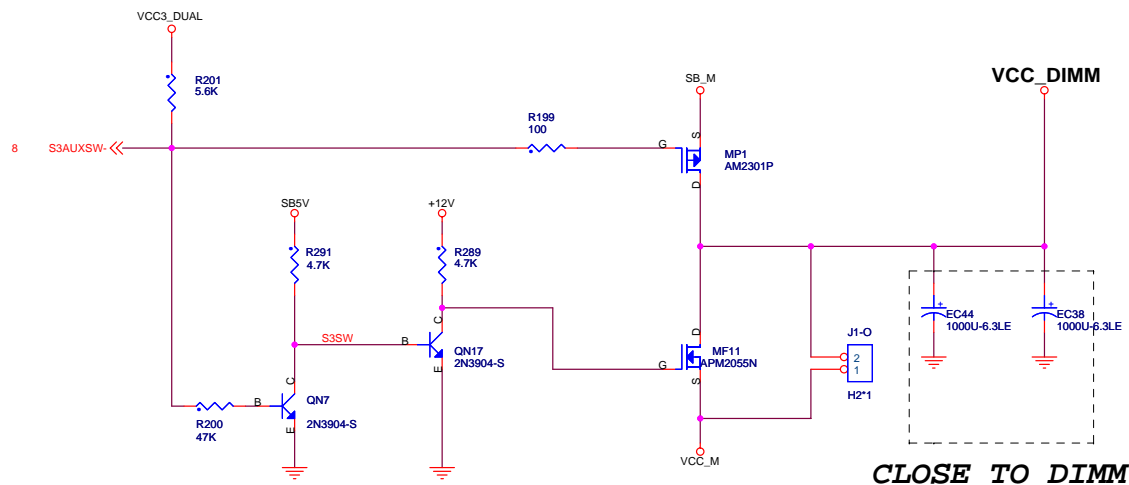
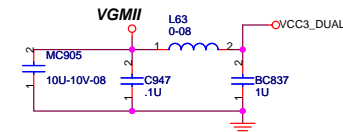
2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

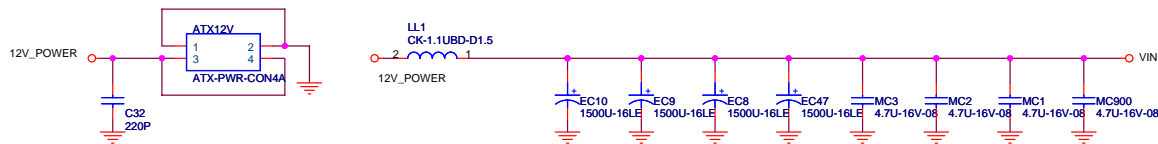
NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER.(ADDITIONAL
500mA PER USB PORT)

VCC3_DUAL & VCC5_DUAL



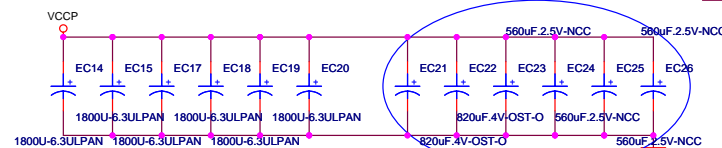
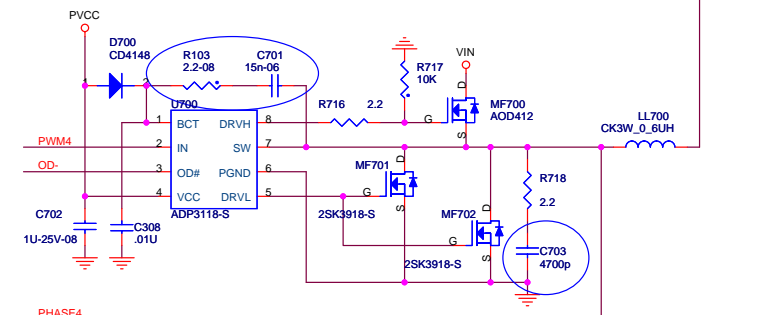
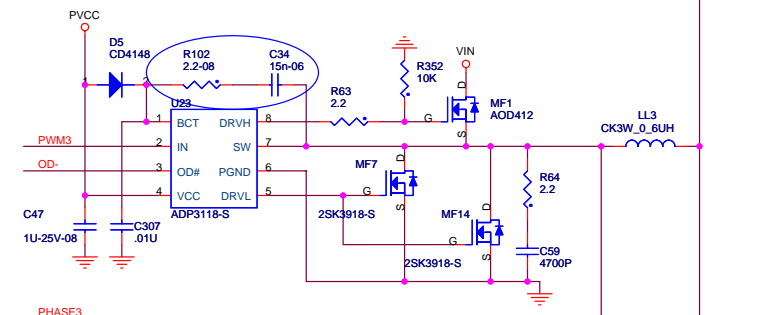
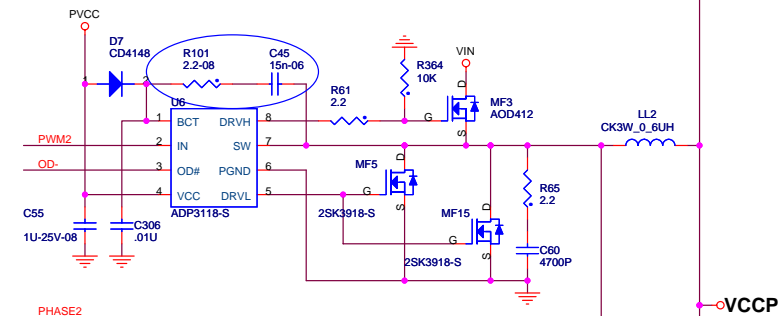
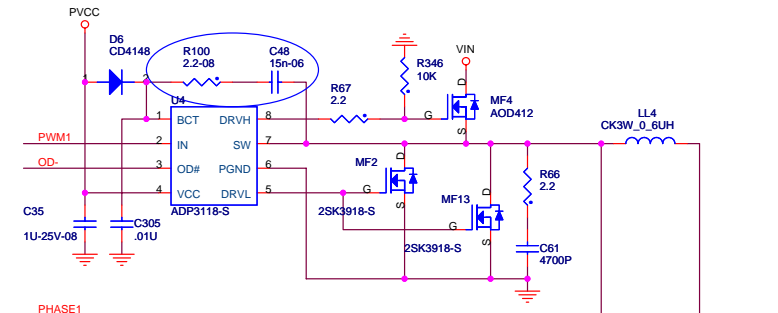
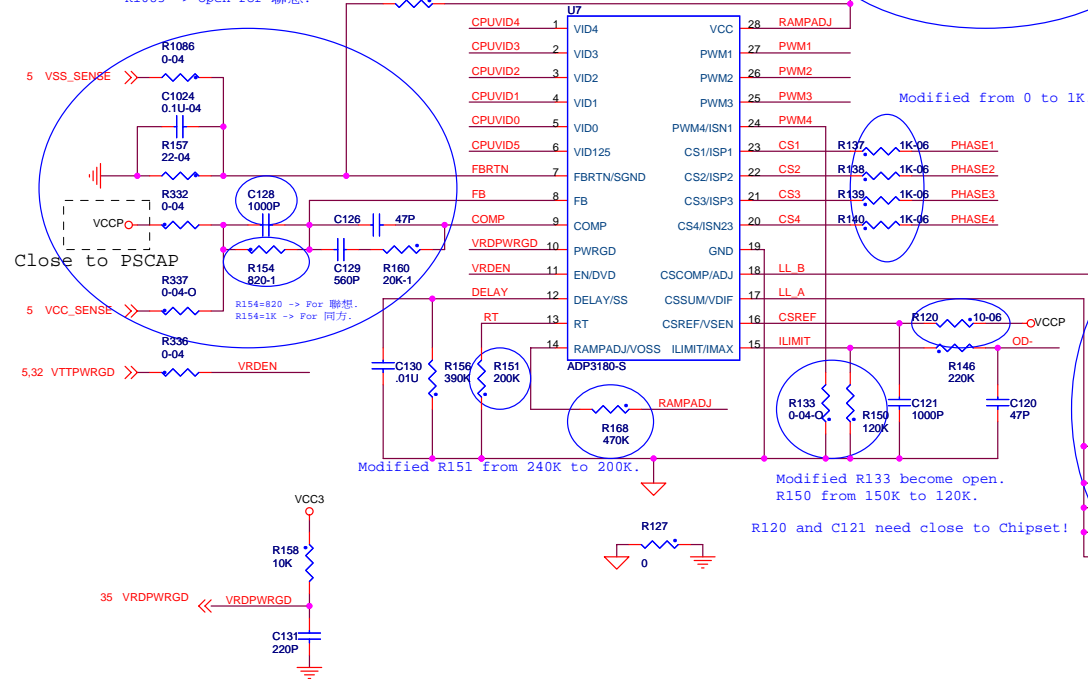
SB1.8V (For SB and DDRII) 800mA

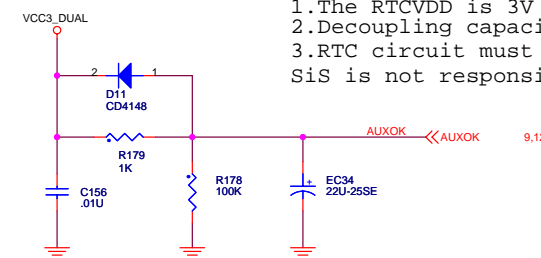
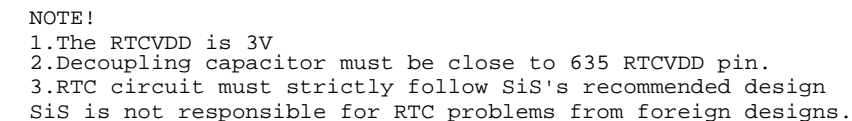
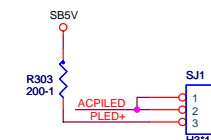
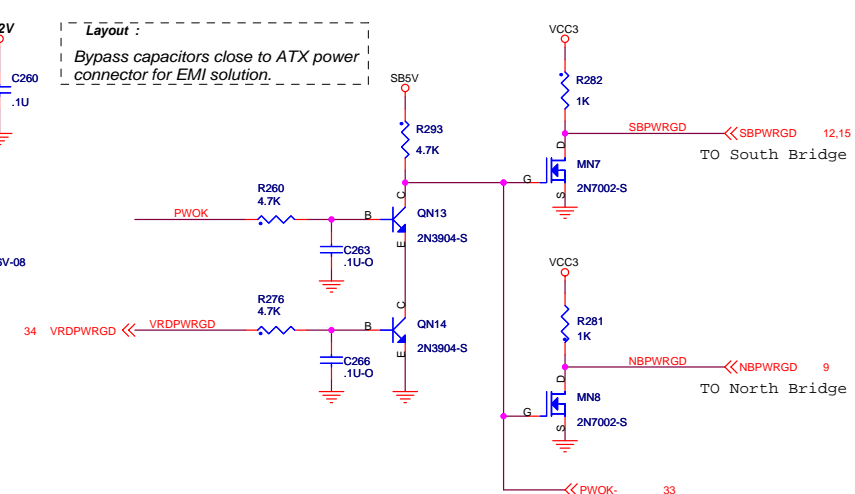




4 CPUVID[0..5] >> CPUVID[0..5]

R157 -> 22 Ohm for TF.
R1085 -> 5.1K Ohm for TF.
R157 -> 0 Ohm for 聯想.
R1085 -> open for 聯想.





1. BOM Attention

(1) South Bridge

Option Components	SIS964	SIS964L
U13	964	964L
R241	374	X
R71, R74	33	X
R72, R75	49.9	X
R331	330	X
D23	1N4148	X
SATA1	O	X
SATA2	O	X

(2) 661FX On-Board VGA

Option Components	Support	No Support
U8	661FX	648FX
L30, L31, L32	FB-120	X
C112, C116, C117, BC35	1U	X
C118, C119	.1U	X
MC36, MC37	10U	X
R136	130	X
R134, R143	33	X
R128, R135	100	X
VGA1	O	X
L6, L7, L8	FB-80	X
C111, C114, C115	22P	X
R22, R23, R24	75	X
R32, R39	2.2K	X
CV1~7	22P	X
F2	O	X
R234	475	169
R248	1K	301
R197	475	374
R198	215	200

(3) LAN

Option Components	8100C 10/100 Mbps	8110S 1Gbps	8110SB 1Gbps	8201BL 10/100 Mbps	8201CL 10/100 Mbps
LAN1	RTL8100C 01-230-100351	RTL8110S 01-230-110350	RTL8110SB	RTL8201BL 02-448-201861	RTL8201CL 02-462-201860
R53	5.6K-1	2.49K-1	2.49K-1	5.9K-1	2K-1
R12, R14, R21, R28	X	49.9	X	X	X
C10, C18	X	0.1u	X	X	X
C52, C53, C54	X	0.01u	X	X	X
C51	0.1u	0.01u	0.01u	X	0.1u
RJ2	X	(1-2) 0 ohm	X	X	(2-3) 0 ohm
R604	X	X	X	X	0 ohm
C601	X	X	X	X	0.1u
L14/ C23	X	0 ohm/ 0.1u	0 ohm/ 0.1u	X	X
RJ7/ C19	(1-2)FB-600 /10u-08	X	(2-3)FB-600 /10u-08	X	X
L21	0 ohm	X	X	0 ohm	0 ohm
QP1	X	HA8550	HA8550	X	X
RJ1	(1-2) 0 ohm	(2-3) 0 ohm	(2-3) 0 ohm	X	X
RJ8	X	X	X	X	(2-3) 0 ohm
QP3	HPN2907A	HA8550	HA8550	X	X
RN601, RN602, RN603	X	X	X	4.7K-8P4R	4.7K-8P4R
C601	X	X	X	0.1u	0.1u
R608/ R609	X	X	X	4.7K/ 10K ohm	4.7K/ 10K ohm
R605	X	X	X	1.5K ohm	1.5K ohm
R602, R603, R607	X	X	X	22 ohm	22 ohm
SR600/ SR601/ SR602/ SR603/ SR607/ SR608	X	X	X	22 ohm-B	22 ohm-B
SR606	150 ohm-B	150 ohm-B	150 ohm-B	X	X
SR604/ SR605	15K/ 1K ohm-B	15K/ 1K ohm-B	15K/ 1K ohm-B	X	X
Y600/ R600	X	X	X	Y-25M/ 0 ohm	Y-25M/ 0 ohm
C166/ C600	4.7K ohm/ X	4.7K ohm/ X	4.7K ohm/ X	22P	22P
R190/ R191	X / 1K ohm	X / 1K ohm	X / 1K ohm	1K ohm/ X	1K ohm/ X
EEPROM1/ EEPROM3	O / X	O / X	O / X	X / O	X / O
R54/ R610	3.6K ohm/ X	3.6K ohm/ X	3.6K ohm/ X	X / 4.7K ohm	X / 4.7K ohm

2. GPIO Function

GPIO		Status	0	1	Jumper
GPIO5	* RESERVED		RESERVED	RESERVED	JPT4
GPIO6	* RESERVED		RESERVED	RESERVED	JPT5
GPIO7	* LAN Selection		LANPHY	PCILAN	
GPIO9	USB, PS/2 S4/S5 Wake Up		Disable	Enable	
GPIO10	DDR Voltage		2.54V	2.63V	
GPIO11	* WHQL		No Support	Support	JPT3
GPIO13	Flash Write Protect		Un-Protect	Protect	

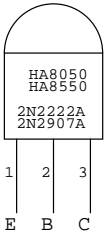
(1) "*" means that the function is selective and ECS may make changes at any time, without notice in this page.

(2) Jumper Setting (Header 3*1):

1: (1-2)


0: (2-3)

(3) Please see Page.12 for more detail jumper function.



CD4148 03-021-214890
(SUB)1N4148W 03-021-214840
(SUB)CDSN4148 03-021-214840

MOS:
AM2301P 03-050-530189 Vds=-20,Vgs=8, Id=-2.3, Rds=130m
AO3413 03-050-541382 Vds=20,Vgs=8, Id=3, Rds=97m
IRLML6402 03-050-540239 Vds=20,Vgs=12, Id=3.7, Rds=65m
APM2023N 03-050-702378 Vds=20,Vgs=12, Id=12.8, Rds=20m
AOD434 03-050-743482 Vds=20,Vgs=12, Id=18, Rds=15m
IPD20N03L 03-050-700359 Vds=30,Vgs=20, Id=30, Rds=20m
P45N02LD 03-050-750359 Vds=25,Vgs=20, Id=45, Rds=20m
APM2055N 03-050-705578 Vds=20,Vgs=16, Id=12, Rds=70m
P3055LD 03-050-705527 Vds=20,Vgs=20, Id=12, Rds=50m
STD1703L 03-050-770345 Vds=30,Vgs=20, Id=17, Rds=50m

Elitegroup Computer Systems

Title649-M3

SizeCustom

Document NumberBOM Attention & GPIO Distribution

DateWednesday, June 15, 2005

Rev1.0

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